# ITRS 2.0 - More Moore update

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On behalf of More Moore Focus Team – Device, Memory, Litho, Interconnect, FEP, Metrology TWGs

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# ITRS 2.0 - More Moore Mission

Provide physical, electrical and reliability requirements for logic and memory technologies to sustain More Moore (PPAC: power, performance, area, cost) scaling for big data, mobility, and cloud (IoT and server) applications and

Forecast logic and memory technologies (15 years) in main-stream/high-volume manufacturing (HVM)

# Cloud and mobile computing drive More Moore

**Big Data**
and abundant computing power are pushing computing to the
**Cloud**

**Instant Data**
generated by sensors and users are pushing computing to the
**Edge**

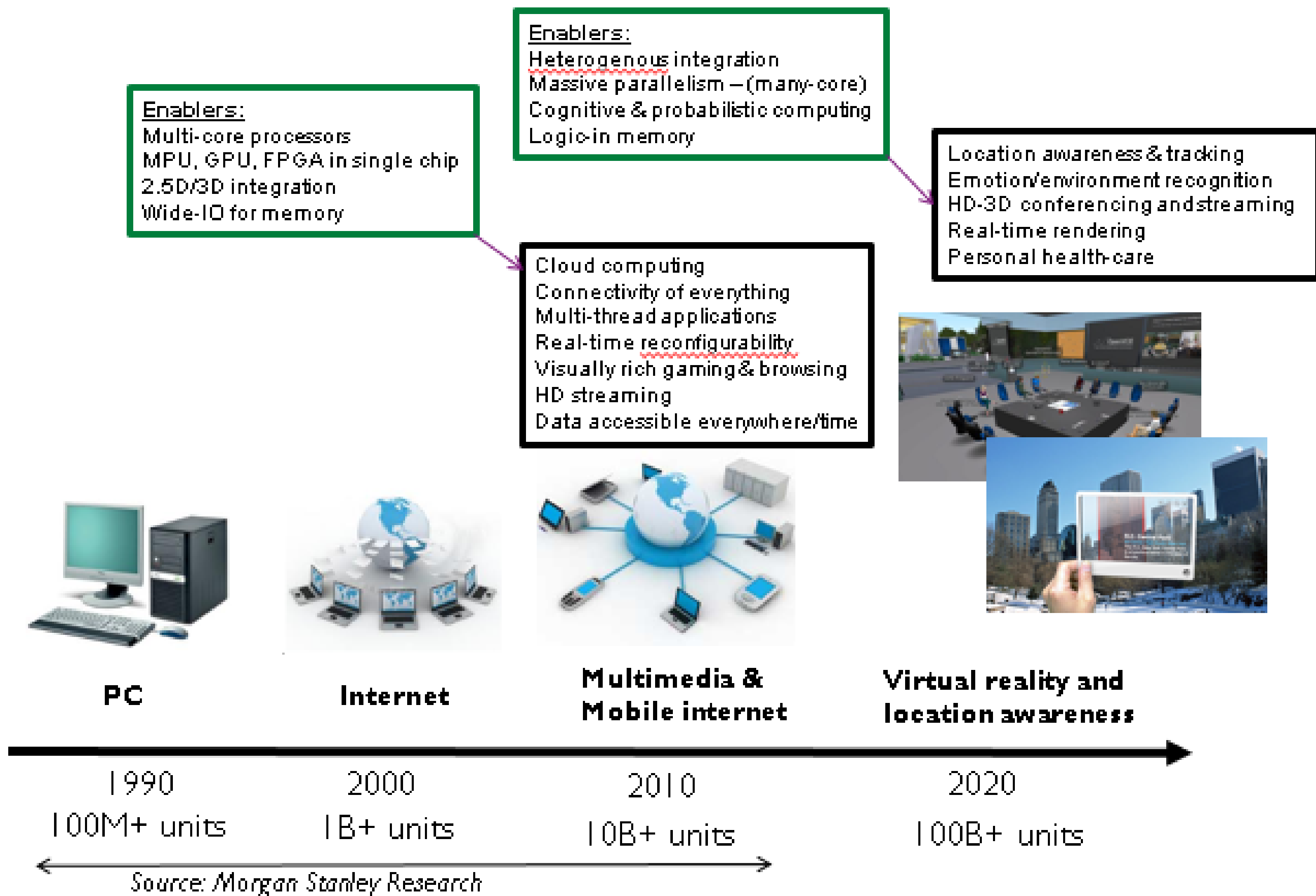
Internet of Things

**Micro (data) servers and memory**

**Mobile computing**

- Device-interconnect tech should meet microserver and mobile computing needs
- Edge computing requires additional functionality for increased consumer value (e.g. motion processor, neural processor unit, etc)
- 2.5D integration to scale memory bandwidth / power and latency

# More Moore computational drivers




**Work in Progress – Not for Distribution**

# Application KPIs and PPAC scaling for More Moore

- **Data/compute servers**
  - KPI = More performance at iso power density
  - Constraints = Thermal, energy budget
- **Edge computing**
  - KPI = More performance & functionality at iso power and cost
  - Constraints = Cost, battery, increased leakage in parallel HW

- **Smart sensors**
  - KPI = Reduced leakage and variability at near-Vt
  - Constraints = System form factor, cost, and security

- **More Moore platform for node-to-node PPAC value**
  - **P**erformance: >25-30%  more fmax @ iso power
  - **P**ower: >50% less energy / switching at given performance
  - **A**rea: >50% area reduction
  - **C**ost: <25% wafer cost – ~30% less cost for same function

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# Performance saturates in conventional scaling

## Saturated performance improvement trend, 2013 ITRS

Speed (CV/I)

CV/I (ps)

100
10
1
0.1
0.01

1980 1990 2000 2010 2020 2030

Year

Intel
IEDM
ITRS
2011 Version
FinFET
FDSOI
2013 ver.
Strain
HKMG
HP
III-V (HP, MG)
ITRS
2011

Energy
($CV^2$, $W_g$=3$L_g$)

$CV^2$ (fJ)

1000
100
10
1
0.1
0.01
0.001

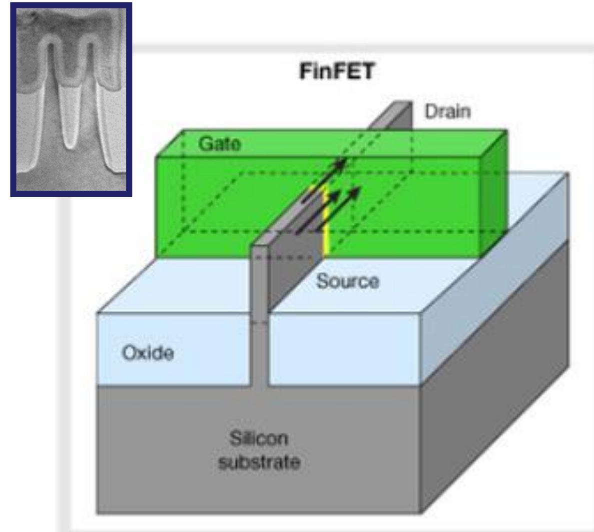
1980 1990 2000 2010 2020 2030

Year

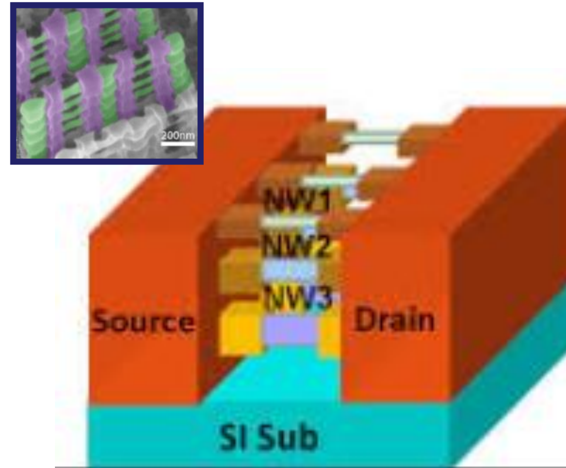
Intel
IEDM
ITRS
2011 Version
FinFET
FDSOI
2013 ver.
Strain
HKMG
HP
III-V (HP, MG)
ITRS
2011

*Source ; Prof. Hiramoto, Tokyo Univ.*

# Device architecture evolution to scale CPP

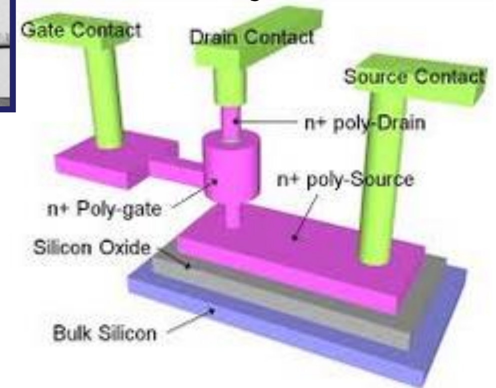



finFET
2011-2019
Lgate/finwidth=3
Weff, SCE

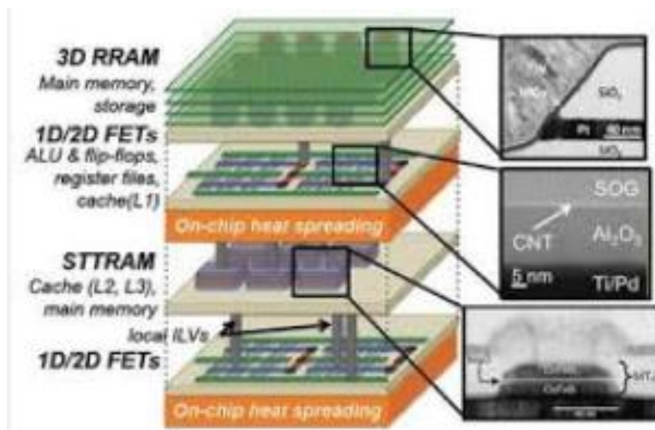



Lateral GAA (gate-all-around)
2018-2024
Lgate/NWD=2
Scale Lgate ~ power reduction

*CPP scaling*
*Variability control*




Vertical GAA
2022-2028
Lgate/NWD=2
Variability control, Rext




Monolithic 3D (M3D)
2024-beyond
Lgate/NWD=2
Functional scaling

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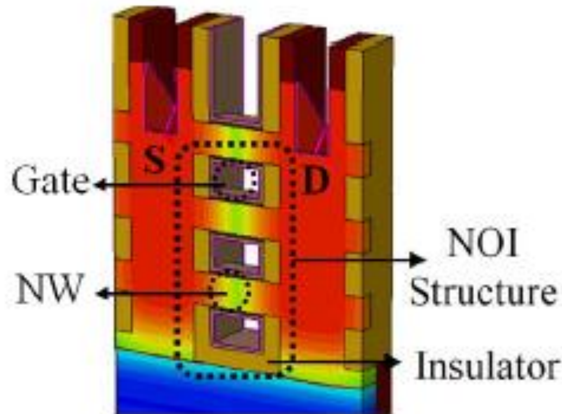
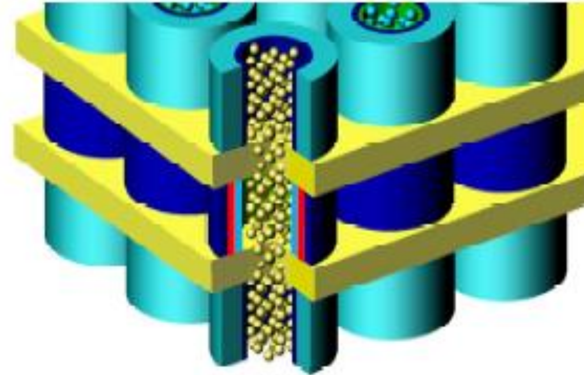
# LGAA and VGAA FEP and metrology challenges

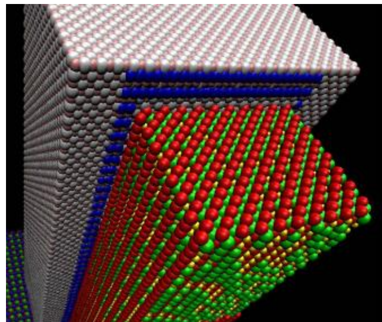



Stacked lateral GAA or NW

S-G. Hur, Samsung



Vertical GAA or NW



Kuhn, Intel, 2012

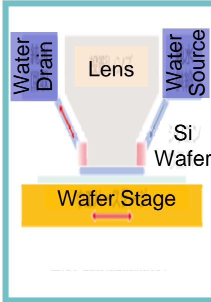
**Stacked NW and GAA structures bring new FEP process challenges**

- Conformality
- Integrity
- Reliability
- Controls
- 3D metrology for sub-10nm
- Defectivity
- Yield

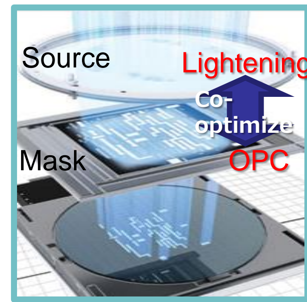
# Technology Roadmap Landscape

45/40nm | 32/28nm | 22/20 nm | 16/14nm | 10nm | 7nm | 5nm ~Beyond

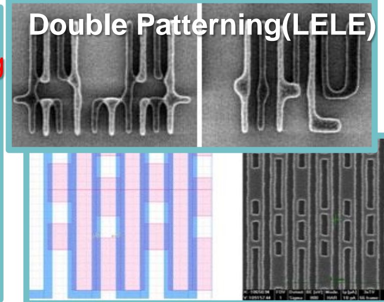
**Litho**



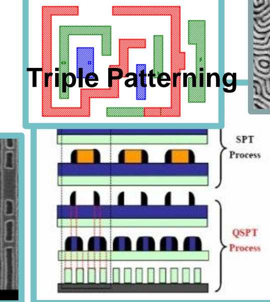

193nm Imm.ArF



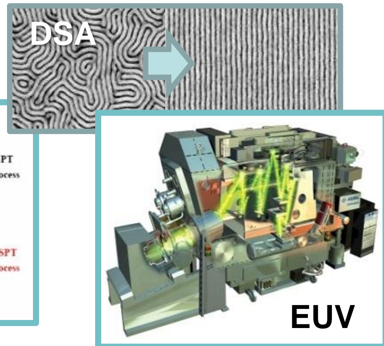

Source Mask Optimization




Double Patterning(SADP)

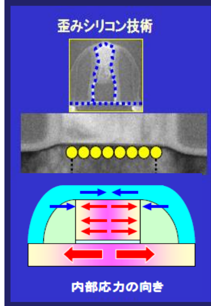



SAQP

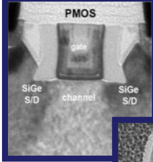



EUV

**Front End**

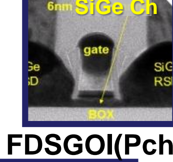



Stress Engineering



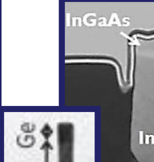

HKMG GL

NMOS SiC:P

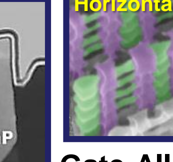



FDSGOI(Pch)

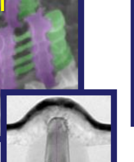
Weff boost Fin FET

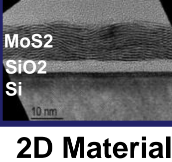



III-V channel

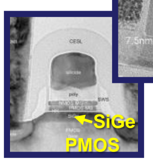



Gate-All -Around

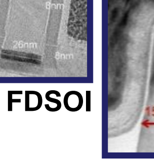


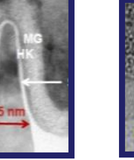

2D Material



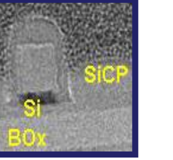

SiGe P-Ch.



FDSOI

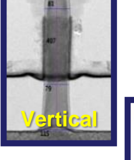



Fin FET



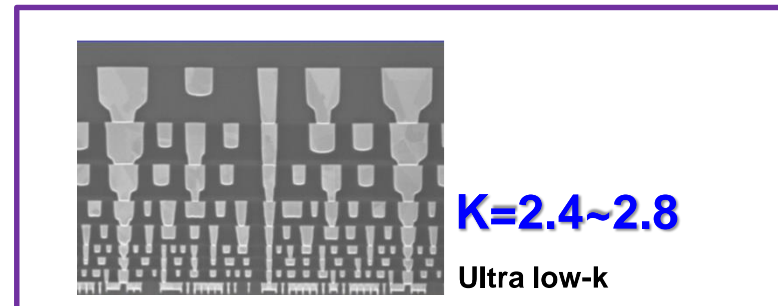

FDSOI(Strain)

Ge channel



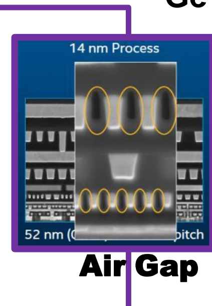
Graphene FET

**Back End**

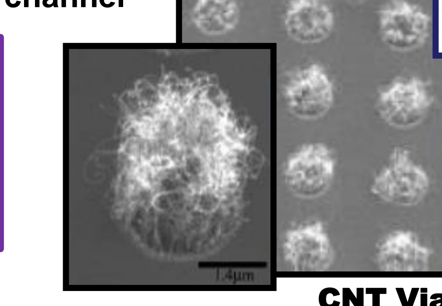


K=2.4~2.8

Ultra low-k




Air Gap




CNT Via

Graphene Wiring

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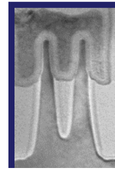
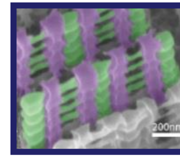
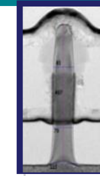
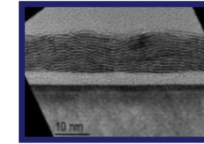
Courtesy: Yuzo Fukuzaki – Sony Corporation

# Main scaling focus & performance boosters

| YEAR OF PRODUCTION | 2015 | 2016 | 2018 | 2020 | 2022 | 2024 | 2026 | 2028 |
|---|---|---|---|---|---|---|---|---|
| *Logic device technology naming* | P70M52 | P52M36 | P42M24 | P32M16 | P24M12 | P24M12V1 | P24M12V2 | P24M12V3 |
| *Logic industry "Node Range" Labeling (nm)* | "16/14" | "11/10" | "8/7" | "6/5" | "4/3" | "3/2.5" | "2/1.5" | "1/0.75" |
| *Node production years* | 3 | 3 | 3 | 3 | 3 | 3 | 3 | >3 |
| *Device structure options* | finFET FDSOI | finFET FDSOI | finFET LGAA | finFET LGAA VGAA | VGAA, M3D | VGAA, M3D | VGAA, M3D | VGAA, M3D |
| **DEVICE ARCHITECTURE & MODULES** | | | | | | | | |
| *N-channel* | Si | sSi | sSi, Ge | sSi, sGe, IIIV | sSi, sGe, IIIV | sSi, sGe, IIIV | sSi, sGe, IIIV | sSi, sGe, IIIV |
| *P-channel* | Si | Si,SiGe | Si,SiGe | Si,SiGe | Ge | Ge | Ge | Ge |
| **DEVICE PERFORMANCE BOOSTERS** | | | | | | | | |
| *Main performance booster* | SCE finHeight Vt | SCE finHeight Vt | Parasitics finHeight | Parasitics finHeight | Low Vdd 3D | Low Vdd 3D | Low Vdd 3D | Low Vdd 3D |
| *Scaling focus* | Perf | Power | Power | Power | Function | Function | Function | Function |
| *Transport scheme* | DD | Quasi Ballistic | Quasi Ballistic | Ballistic | Ballistic TFET, JFET, NCMOS | Ballistic TFET, JFET, NCMOS | Ballistic TFET, JFET, NCMOS, Spin | Ballistic TFET, JFET, NCMOS, Spin |

- Added new node naming nomenclature (e.g. P70M52) since pitch scaling is not directly representing node itself
- 2014-2018 (N14, N10) focus on SCE, Weff scaling through cell height reduction
- 2018-2022 (N7 and N5) focus on parasitics, Weff efficiency, DTCO
- 2022-2030 (N3 and beyond) focus on ultra low-Vdd and 3D functional integration

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# Inflection (2018) - Lateral GAA transition

- Benefits
  - Strong short channel control – high beneficial in loaded cells
  - Can use the finFET baseline as process starting point
- Technology challenges
  - Undercut control during channel formation
  - HKMG integration surrounding NW
  - Parasitic channel
  - Stressor to mobility transfer
  - Conformal deposition
- Design challenges
  - Self-heating
  - Enabling SoC components – ESD, IO
  - Variability

# Inflection (2022) - Vertical GAA transition

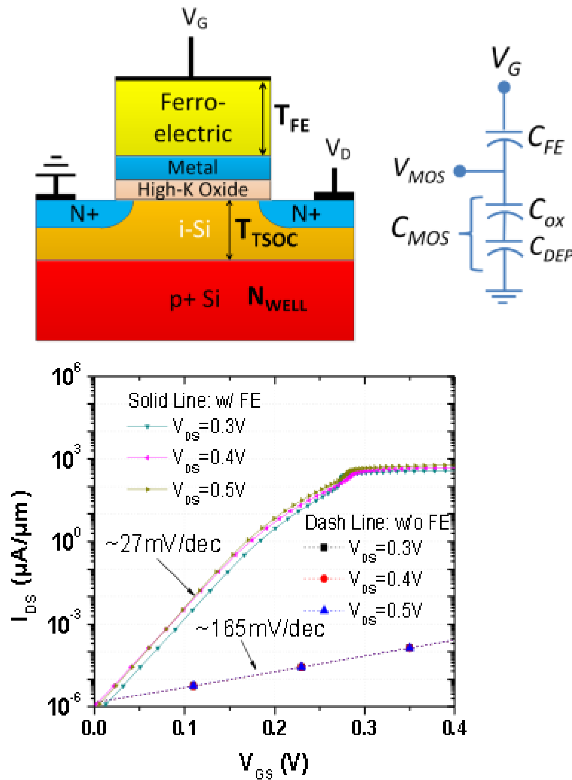
- Benefits
  - Strong short channel control – high beneficial in loaded cells
  - No need for isolation
  - Reduced SRAM area
- Technology challenges
  - Etch control
  - HKMG integration surrounding NW – easier compared to finFET
  - Bottom contact formation
  - Bottom junction engineering
- Device/Design challenges
  - Gate density
  - Same as lateral nanowire
  - 3D stdcell design & port access difficulties
  - Place & route

# Inflection (2022) - monolithic-3D transition

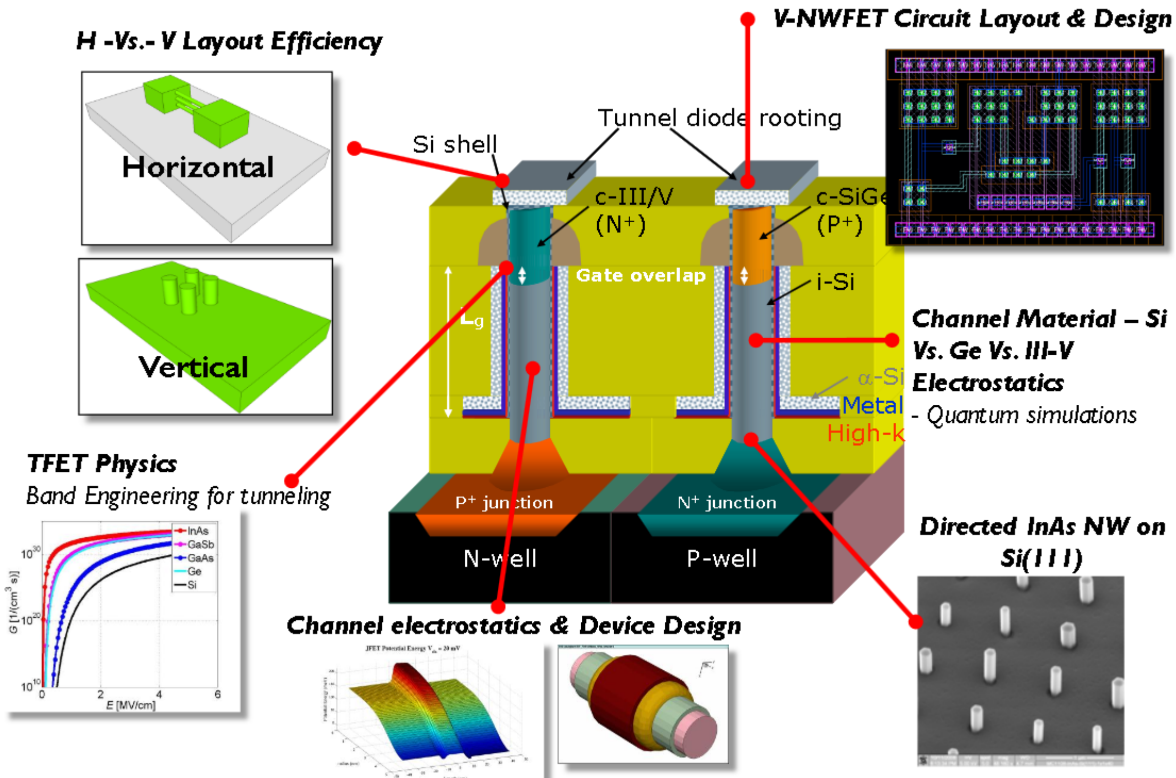
- Benefits
  - Strong short channel control – high beneficial in loaded cells
  - No need for isolation
  - Active devices in the interconnect
  - Ability to scale drive in the vertical direction
  - P-N separation across tuers
- Technology challenges
  - Same as vertical nanowire
  - Temperature budget
  - Channel growth
  - Low-temperature activation
- Device/Design challenges
  - New functions and architectures
  - Same as vertical nanowire
  - 3D stdcell design & port access difficulties
  - Less number of layers across tiers
  - Place & route

# Lgate slow-down forcing alt. transport

## NCFET




## TFET

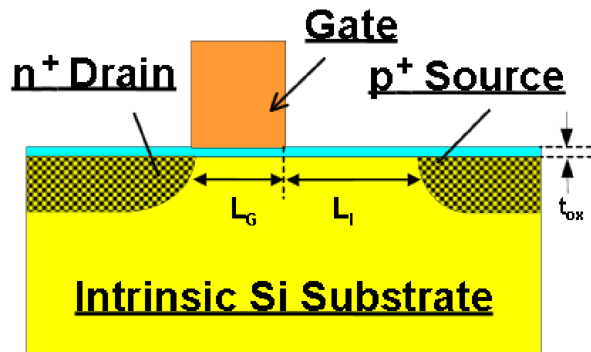


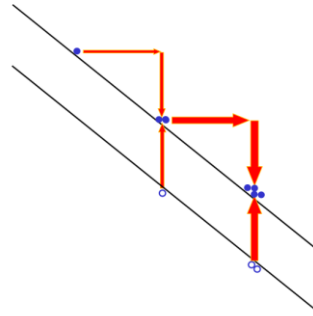

[Source: Yeung (UCB), SISPAD 2012]

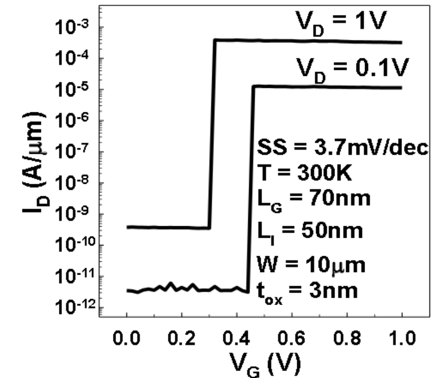
[Source: Thean (imec), ITF 2013]

# Other transport options

## IMOS



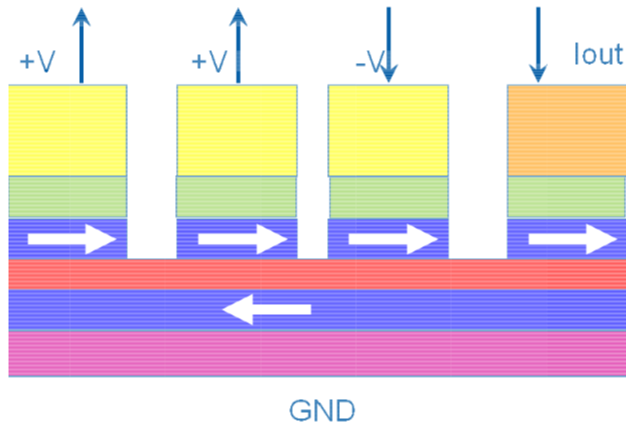


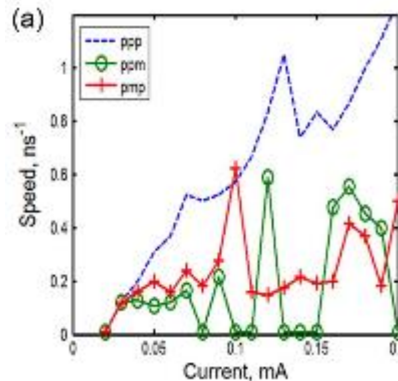

<n-channel I-MOS>

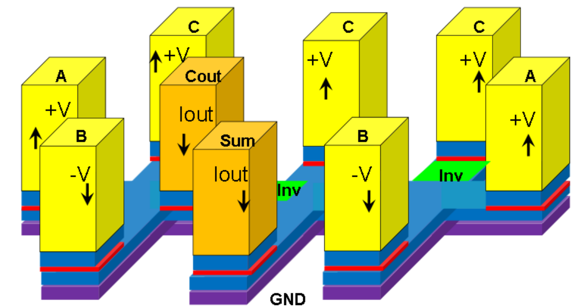
<n-channel I-MOS>

*[Source: Gopalakrishnan (Stanford U.), IEDM 2002]*

## STMG




***Full Adder***

*[Source: Nikonov (Intel), IEEE EDL 2011]*

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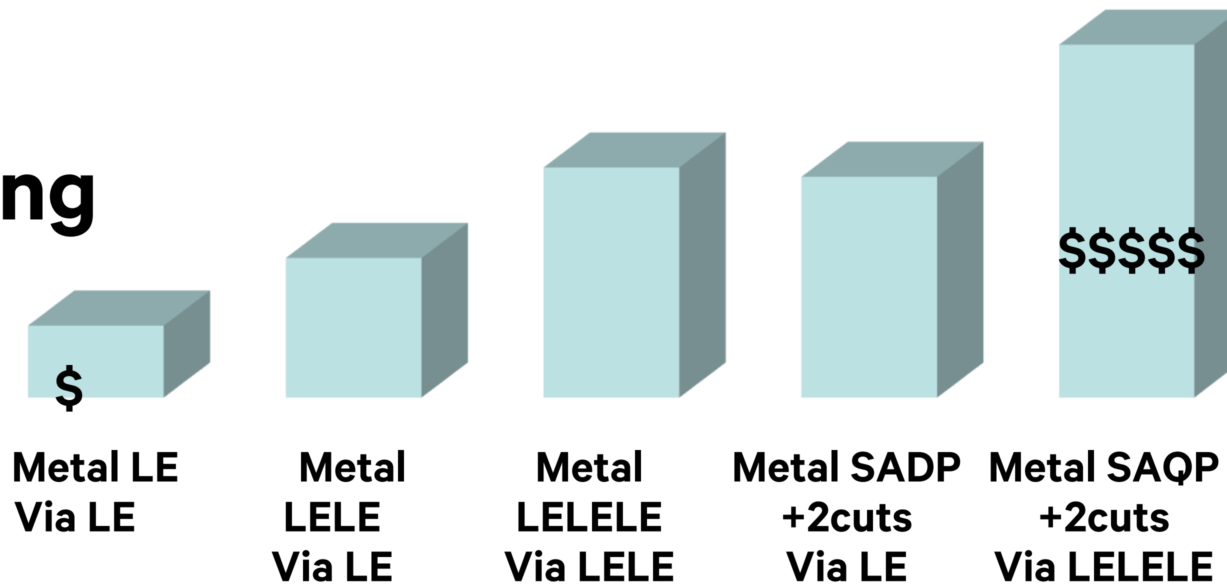
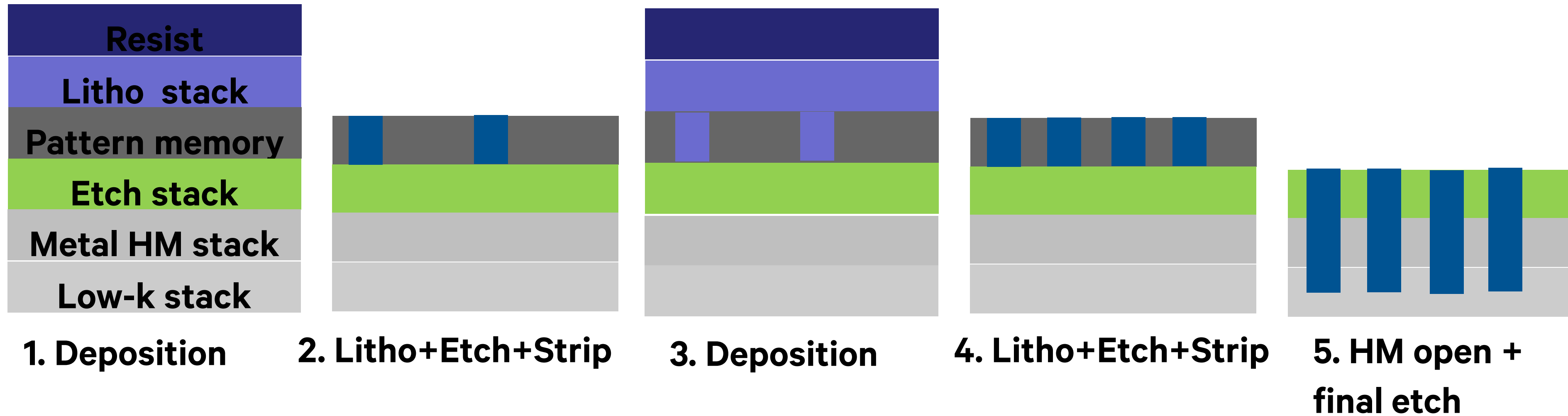
# 193i multi-patterning cost explosion




***Need for 193i litho stack simplification through innovative materials***

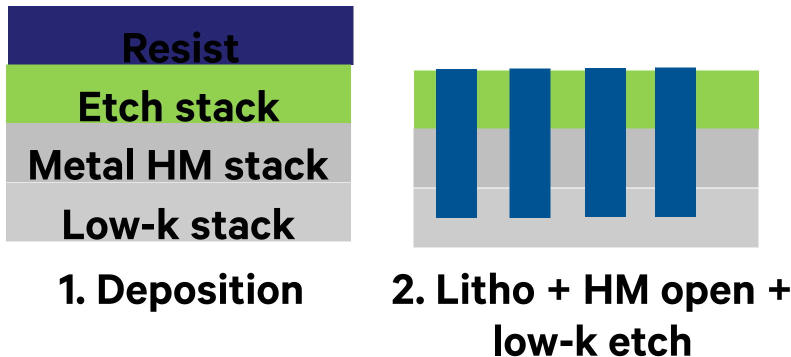
# EUV - simplifying stack and saving steps

## 193i LELE metal patterning




1. Deposition
2. Litho+Etch+Strip
3. Deposition
4. Litho+Etch+Strip
5. HM open + final etch

## EUV SE metal patterning




1. Deposition
2. Litho + HM open + low-k etch

Pros
- Simplified stack
- Avoiding CDU and OVL seen in MPT
- Less # of depo, litho, etch steps

Cons
- Need improvements in resists for productivity and better LER

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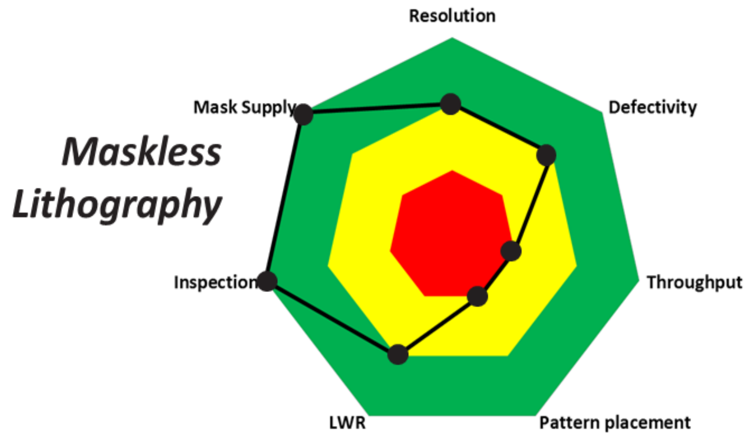
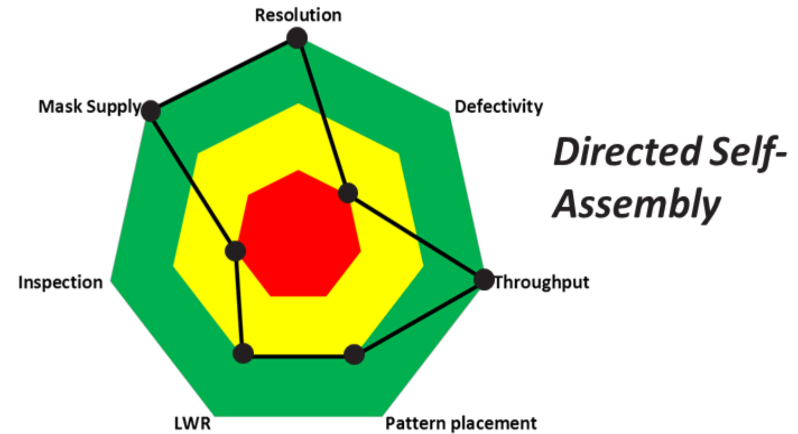
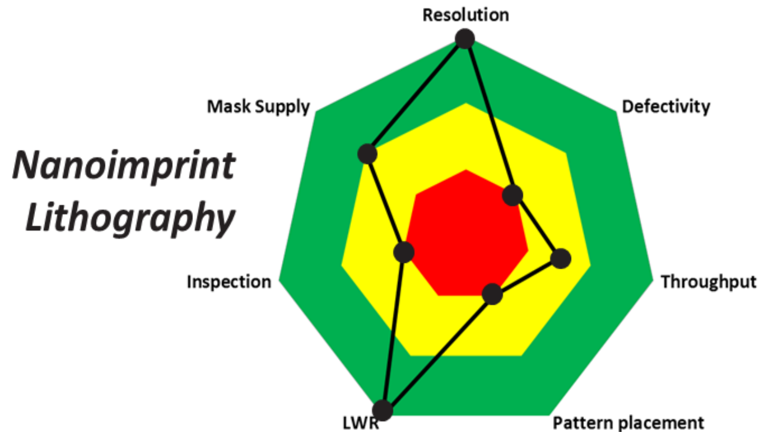
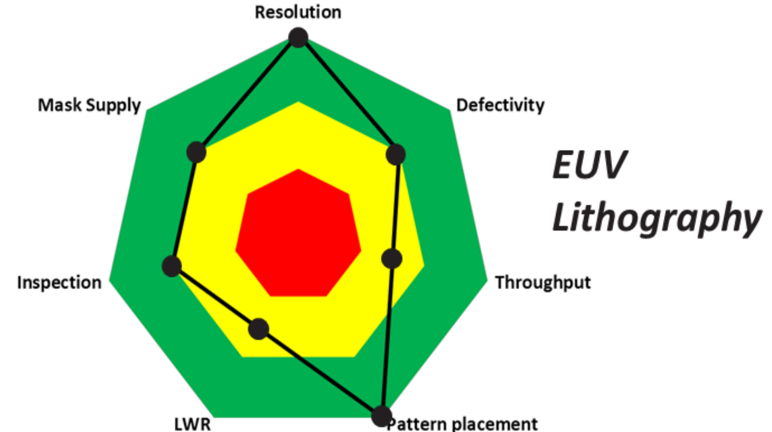
# Pros/cons of patterning approaches




**Courtesy: Mark Neisser - Sematech**

# Interconnect – new barriers, conductors

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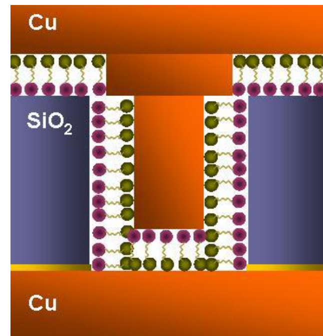
| Node production years | 3 | 3 | 3 | 3 | 3 | 3 | 3 | >3 |
| Device structure options | finFET FDSOI | finFET FDSOI | finFET LGAA | finFET LGAA VGAA | VGAA, M3D | VGAA, M3D | VGAA, M3D | VGAA, M3D |
| INTERCONNECT TECHNOLOGY | | | | | | | | |
| Conductor | Cu | Cu | Cu | Cu Silicides Carbon Collective Excitations | Cu Silicides Carbon Collective Excitations | Cu Silicides Carbon Collective Excitations | Cu Silicides Carbon Collective Excitations | Cu Silicides Carbon Collective Excitations |
| Number of wiring layers | 10 | 11 | 12 | 13 | 15 | 17 | 19 | 21 |
| Barrier metal - intermediate wire (tight pitch) | Ta(N) | Ta(N), Mn(N) | Ta(N), Mn(N) | Ta(N), Mn(N), SAM | Ta(N), Mn(N), SAM | Ta(N), Mn(N), SAM | Ta(N), Mn(N), SAM | Ta(N), Mn(N), SAM |
| Barrier thickness - intermediate wire | | | | | | | | |
| Inter-metal dielectrics (IMD) and k value - intermediate wire | SiCOH (2.55) | SiCOH (2.40-2.55) Airgap (1.0) | SiCOH (2.20-2.55) Airgap (1.0) | SiCOH (2.20-2.55) Airgap (1.0) MOF, COF | SiCOH (2.00-2.55) Airgap (1.0) MOF, COF | SiCOH (2.00-2.55) Airgap (1.0) MOF, COF | SiCOH (2.00-2.55) Airgap (1.0) MOF, COF | SiCOH (2.00-2.55) Airgap (1.0) MOF, COF |

# Enablers for resistance reduction

Proposals from ERM TWG

## Ultrathin Cu Barrier Layers

### (1) SAM(Self-assembled Monolayer)




NH2(CH2)3Si (OCH3)3

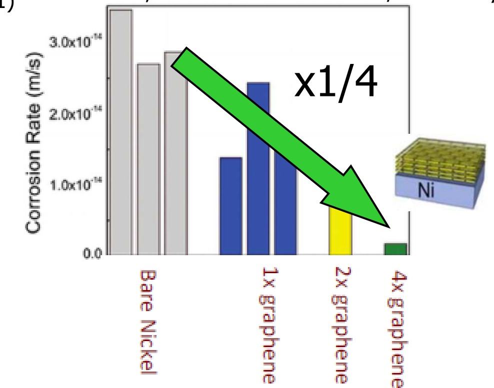
Source: Arantxa Maestre Caro, Intel Corp. at IMEC

### (2) Graphene barrier

Oxidation and corrosion resistance

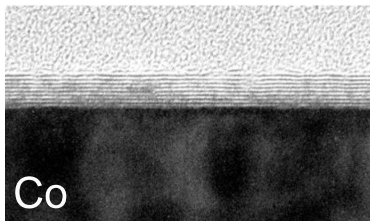
Chen et al., ACS Nano 5, 1321 (2011)

Prasai et al., ACS Nano DOI: 10.1021/nn203507y (2011)

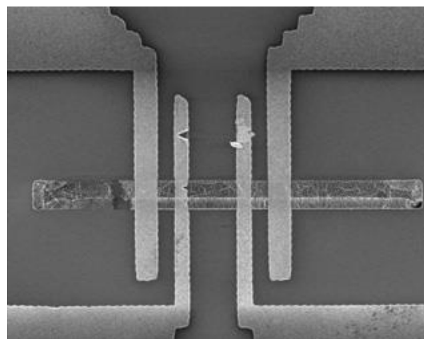


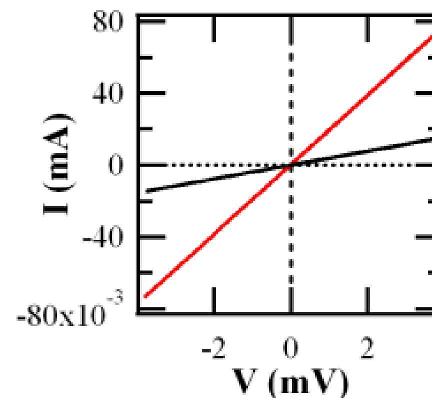

## Alternative Conductors

### (3) Graphene




Kondo et al., IITC2013






9.1 μΩcm at 6 μm length and 4 μm width

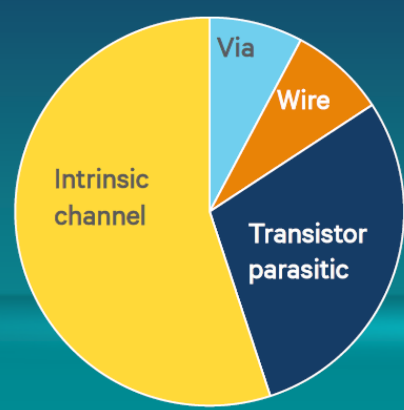
### (4) Other candidates

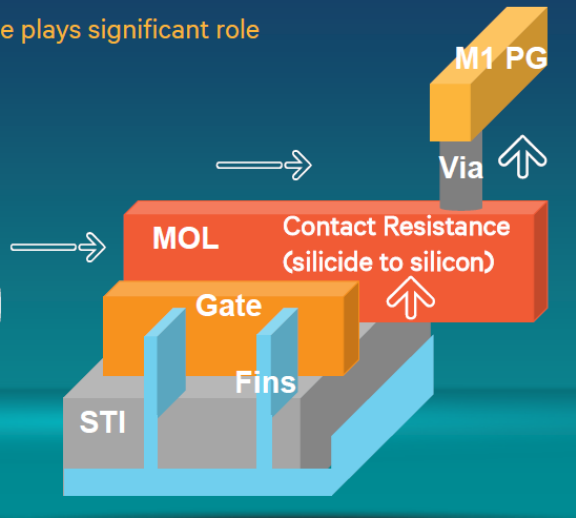
- CNT Interconnects
- CNT-Cu composites

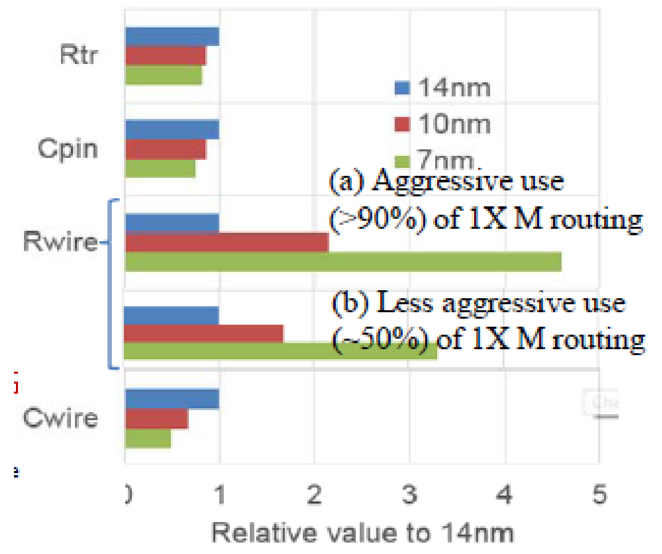
**Work in Progress – Not for Distribution**

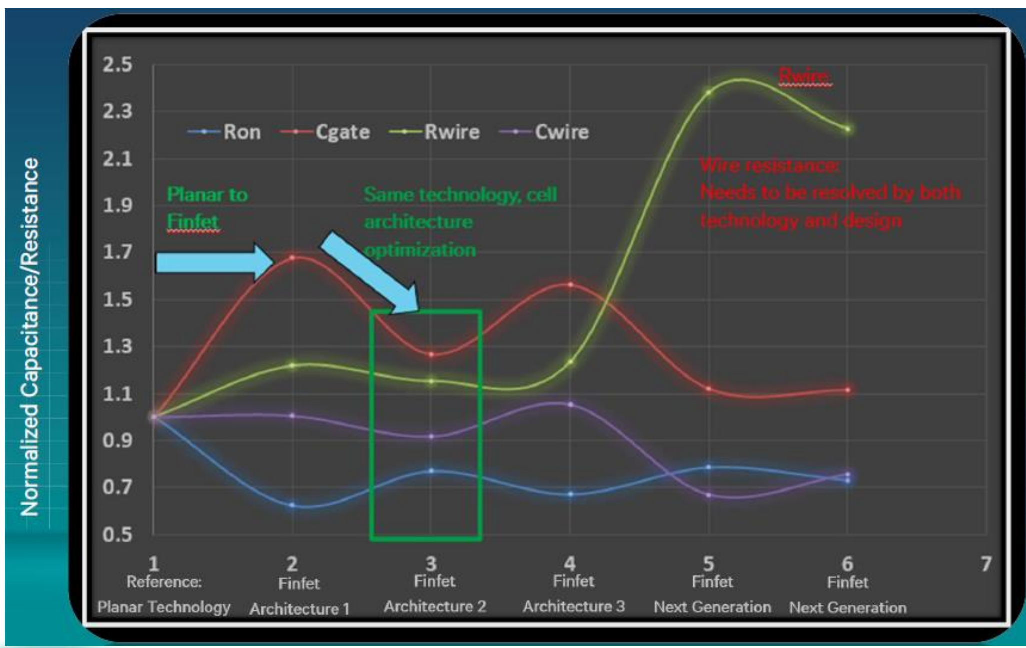
# Transistor drive needs to be optimized

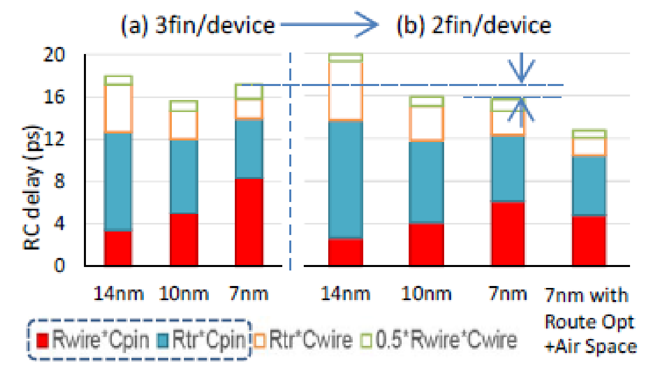
Both BEOL and MOL parasitic resistance plays significant role




**Source: SC Song (Qualcomm), VLSI 2015**

**Source: Terzioglu (Qualcomm), ICICDT 2015**

# Memory scaling wall image

**Memory status On 2015**

- DRAM is still continue to scale in spite of facing the device physics limit on 2D.
- NAND Flash moved to next stage. Now process is constrain for further scaling.
- NOR-Flash scaling is almost stop just before device physics limitation.
- MRAM scaling is on going.
- CRAM/ReRAM scaling is on going but simultaneously 3D

ITRS2.0
Inspection leadership
Unit Process leadership
ITRS1.0
NAND
DRAM
Device physics leadership
Lithography leadership
MRAM
PCRAM
ReRAM
Contamination wall
Lithography wall
Device physics wall
Process technology wall
Inspection technology wall
One or more unknown wall
Investment power wall
Immersion ArF /EUV
Double patterning/Sidewall assisted patterning
3D array
Self-assemble? etc.
???
NOR
Industry Growth
Timeline

**Courtesy: Hirofumi Inoue, Toshiba**

**Work in Progress – Not for Distribution**

# eDRAM size trend – MRAM potential >2019 for L4

eDRAM Half pitch(real F for cell design) = same F/Node definition as DRAM

210 130 130 110 70 57 47 38

Cell Size, $um^2$

1
0.1
0.01
0.001

0.5632
0.3604
0.1848
0.11
0.069
0.0581
0.0583
394
0.029
0.026
0.0174
0.0113

Intel

FinFET eDRAM
* Photo 22nm

Power7
Power7+
Power8

Capacitors under Bitline (CUB)
310nm
Passing Wordline (~55 nm)
Access Transistor (~110 nm)
TSMC
* Photo 65nm

Passing WL
WL
BL
Strap
Pass Device
BOX
Node
Deep Trench Cap
IBM
SOI eDRAM
* Photo 45nm

180 130 90 65 45 32 22 14 10

Process Node(Logic)

- IBM
- Sony/Toshiba
- TSMC
- Intel
- 8F2
- 30F2
- 60F2

**Courtesy: Yuzo Fukuzaki, Sony Corp.**

**Work in Progress – Not for Distribution**

# Conclusions

- Mobile computing, big data, cloud (microserver, IoT) will continue to drive low power technology and design
- New materials needed to resolve the interconnect bottleneck but lack of disruptive solutions, more design solutions for mitigation
- Memory scaling key for the server market handling big data
- NVM scaling requires new memory technologies (e.g. MRAM, RRAM) and embedded memories for IoT
- More Moore - ITRS2.0 focusing on requirements and mitigation approaches/gaps to sustain