EE222 Lecture #1 Jan 9, 2018

Instructor Steve Kang (http://nisl.soe.ucsc.edu)

Website https://ee222-winter18-01.courses.soe.ucsc.edu

Webcast https://webcast.ucsc.edu (EE 222)

Syllabus – see the website

HWs assigned, not collected

1st Midterm Feb. 6 (35%)

project proposal due on Feb. 6

2nd Midterm March 8 (35%)

Presentations March 13, 15 (30%)

10% presentation; 20% written report

Textbook: CMOS Digital Integrated Circuits Analysis & Design, Steve Kang UCSC EE version

Ref 1: Jan Rabaey, Low Power Design Essentials, Springer 2009

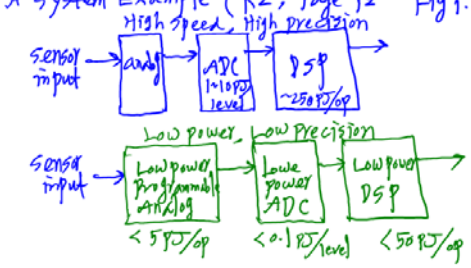
Ref 2: Rahul Sarpeshkar, Ultra Low Power Bioelectronics, Cambridge Univ. Press 2010

Today's coverage Text chap 1 (HW prob 1-1 ~ 1-3)

Ref 1 pp 1~23

Ref 2 pp 1~27

A System Example (R2, Page 12 Fig 1.2)



Why Worry About Power?

The Tongue-in-Cheek Answer

- Total energy of Milky Way galaxy: 10^{59} J
- Minimum switching energy for digital gate (1 electron@100 mV): 1.6×10^{-20}J (limited by thermal noise)

- Upper bound on number of digital operations: 6×10^{78}
- Operations/year performed by 1 billion 100 MOPS computers: 3×10^{24}
- Entire energy might be consumed in **180 years**, assuming a doubling of computational requirements every year (Moore's Law).

(Ref 1)

Power: The Dominant Design Constraint (1)

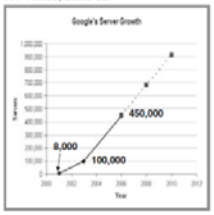
Cost of large data centers solely determined by power bill …

Google Data Center, The Dalles, Oregon

- 400 Millions of Personal Computers worldwide (Year 2000)
  - Assumed to consume 0.16 Tera (10^{12}) kWh per year
  - Equivalent to 26 nuclear power plants
- Over 1 Giga kWh per year just for cooling
  - Including manufacturing electricity

[Ref. Bar-Cohen et al., 2000]

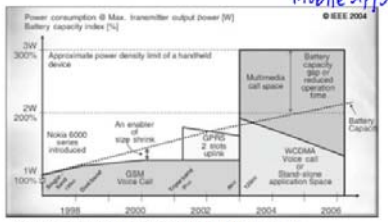
NY Times, June 06



(Ref. 1)

Power : The Dominant Design Constraint (2)

Mobile Apps

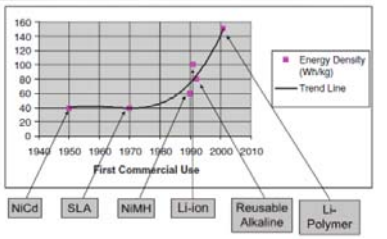


Power consumption and battery capacity trends

[Ref: Y. Nuevo, ISSCC'04]

(Ref. 1)

Battery Evolution



Accelerated since the 1990s, but slower than IC power growth.

(Ref. 1)

Power: The Dominant Design Constraint (3)

Exciting emerging applications requiring "zero-power"

Example: Computation/communication nodes for wireless sensor networks

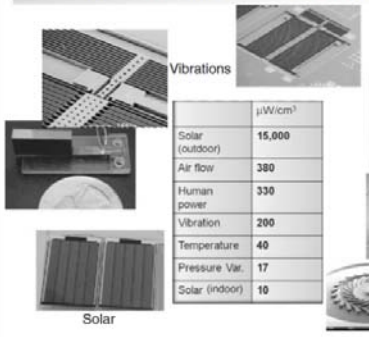
Meso-scale low-cost wireless transceivers for ubiquitous wireless data acquisition that

- are fully integrated
  - size smaller than 1 cm³
- are dirt cheap
  - at or below 1$
- minimize power/energy dissipation
  - limiting power dissipation to 100 µW enables energy scavenging, and
- form self-configuring, robust, ad hoc networks containing 100s to 1000s of nodes

[Ref: J. Rabaey, ISSCC'01]

(Ref. 1)

How Much Energy Can One Scavenge in 1 cm³?



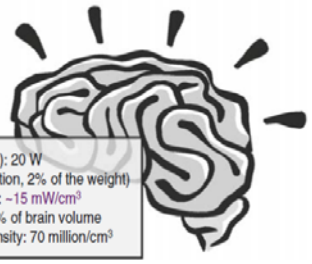
	µW/cm³
Solar (outdoor)	15,000
Air flow	380
Human power	330
Vibration	200
Temperature	40
Pressure Var.	17
Solar (indoor)	10

(Ref.1)

Bio-inspired low-power nanoelectronics

A Side Note: What Can One Do with 1 cm³?

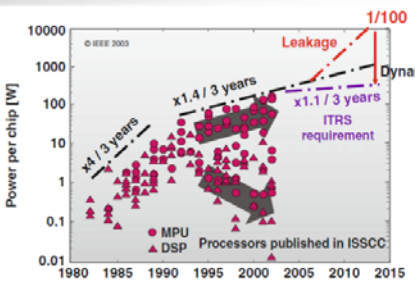
Reference case: the human brain



P_{avg}(brain): 20 W
(20% of the total dissipation, 2% of the weight)
Power density: ~15 mW/cm³
Nerve cells only 4% of brain volume
Average neuron density: 70 million/cm³

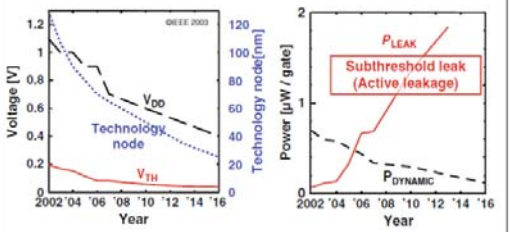
(Ref. 1)

Static Power (Leakage) May Ruin Moore's Law



[Ref: T. Sakurai, ISSCC'03]

Sub-threshold Leakage as an Extra Complication

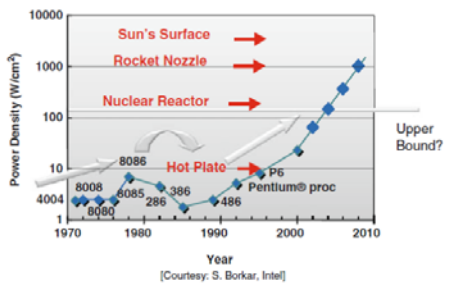


[Ref: T. Sakurai, ISSCC'03]

(Ref. 1)

Power Density Increases

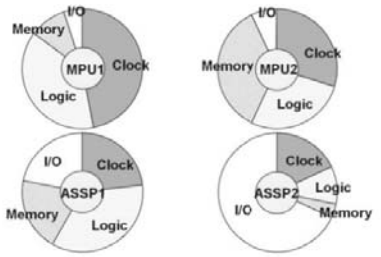
Unsustainable in the long term



[Courtesy: S. Borkar, Intel]

(Ref 1)

Complicating the Issue: The Diversity of SoCs

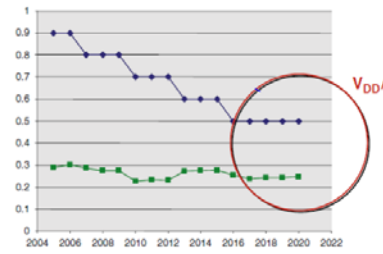


Power budgets of leading general purpose (MPU) and special purpose (ASSP) processors

[Ref: many combined sources]

(R 1)

Supply and Threshold Voltage Trends



Voltage reduction projected to saturate

Optimistic scenario – some claims exist that V_{DD} may get stuck around 1 V

[Ref: ITRS 05, Low power scenario]

(R1)

An Era of Power-Limited Technology Scaling

Technology innovations offer some relief

- Devices that perform better at low voltage without leaking too much

But also are adding major grief

- Impact of increasing process variations and various failure mechanisms more pronounced in low-power design regime

Most plausible scenario

- Circuit- and system-level solutions essential to keep power/energy dissipation in check
- Slow down growth in computational density and use the obtained slack to control power density increase
- Introduce design techniques to operate circuits at nominal, not worst-case, conditions

(R1)