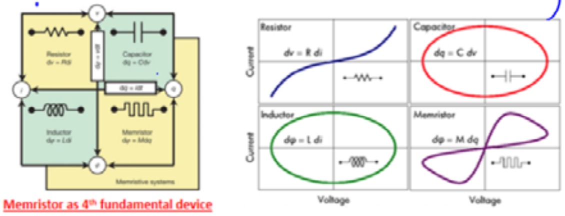
EE 222 Lecture 10 Feb 15, 2018

On Memristors.



Memristor as 4th fundamental device

The first conceptual paper on memristor was by Leon Chua in 1971.

The Missing Link in Constitutive Relations

- Q = **C** V (Capacitor)
- V = **R** I (Resistor)
- Φ = **L** I (Inductor)

?……………………?

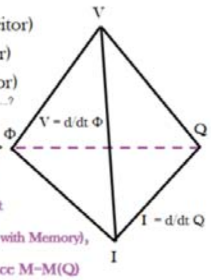
- Φ = f (Q)

dΦ /dt= df(Q)/dt

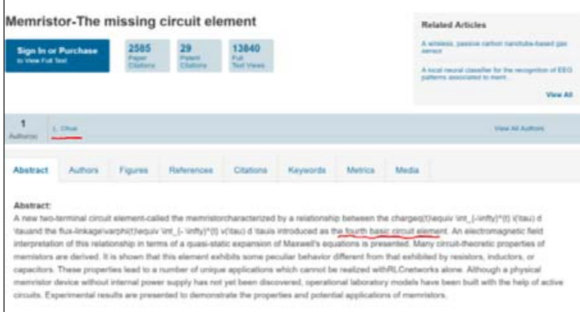
= df(Q)/dQ. dQ/dt

V= M I (Resistance with Memory),

Thus Memristance M=M(Q)



- **Capacitor (1745)** by Ewald Georg von Kleist
- **Resistor (1827)** by Georg Simon Ohm
- **Inductor (1831)** by Michael Faraday



Memristor-The missing circuit element

Abstract:

A new two-terminal circuit element-called the memristorcharacterized by a relationship between the chargeq(t)\equiv \int_{-\infty}^{t} i(\tau) d \tauand the flux-linkage\varphi(t)\equiv \int_{- \infty}^{t} v(\tau) d \tauis introduced as the fourth basic circuit element. An electromagnetic field interpretation of this relationship in terms of a quasi-static expansion of Maxwell's equations is presented. Many circuit-theoretic properties of memistors are derived. It is shown that this element exhibits some peculiar behavior different from that exhibited by resistors, inductors, or capacitors. These properties lead to a number of unique applications which cannot be realized withRLCnetworks alone. Although a physical memristor device without internal power supply has not yet been discovered, operational laboratory models have been built with the help of active circuits. Experimental results are presented to demonstrate the properties and potential applications of memristors.

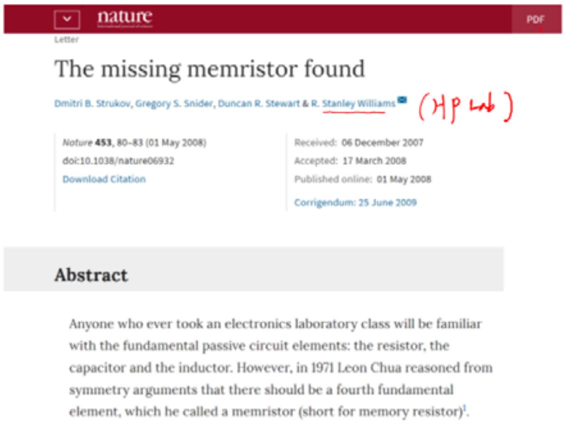
IEEE Trans. on Circuit Theory, Sept. 1971

Memristive devices and systems

Abstract:

A broad generalization of memristors--a recently postulated circuit element--to an interesting class of nonlinear dynamical systems called memristive systems is introduced. These systems are unconventional in the sense that while they behave like resistive devices, they can be endowed with a rather exotic variety of dynamic characteristics. While possessing memory and exhibiting small-signal inductive or capacitive effects, they are incapable of energy discharge and they introduce no phase shift between the input and output waveforms. This zero-crossing property gives rise to a Lissajous figure which always passes through the origin. Memristive systems are hysteretic in the sense that their Lissajous figures vary with the excitation frequency. At very low frequencies, memristive systems are indistinguishable from nonlinear resistors while at extremely high frequencies, they reduce to linear resistors. These anomalous properties have misled and prevented the identification of many memristive devices and systems-including the thermistor, the Hodgkin-Huxley membrane circuit model, and the discharge tubes. Generic properties

Proc. of the IEEE, Feb. 1976
Chua & Kang



Letter

The missing memristor found

Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart & R. Stanley Williams (HP Lab)

Nature **453**, 80–83 (01 May 2008)
doi:10.1038/nature06932
Download Citation

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Corrigendum: 25 June 2009

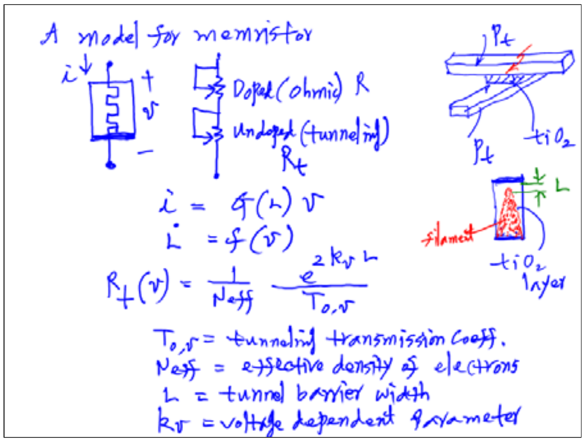
Abstract

Anyone who ever took an electronics laboratory class will be familiar with the fundamental passive circuit elements: the resistor, the capacitor and the inductor. However, in 1971 Leon Chua reasoned from symmetry arguments that there should be a fourth fundamental element, which he called a memristor (short for memory resistor)[1].

Reference

I. Vourkas and G. Sirakoulis,
Memristor-Based Nanoelectronic Computing Circuits and Architecture
Springer, 2016

- Memristor fundamentals
- Memristor modeling
- Dynamic response of Interconnected Memristors
- Memristor-based Logic Circuits
- Memristor Cross-bar based Nonvolatile Memory
- High-Radix ALU based on memristors, etc.



A model for memristor

$i = g(L)\,v$

$\dot{L} = f(v)$

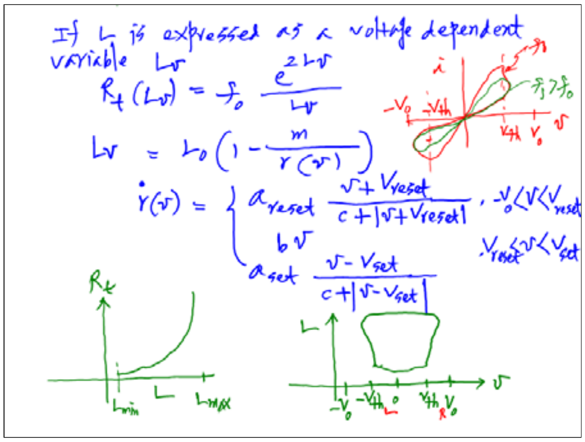
$R_t(v) = \frac{1}{N_{eff}} \frac{e^{2k_v L}}{T_{o,v}}$

$T_{o,v}$ = tunneling transmission coeff.

N_{eff} = effective density of electrons

L = tunnel barrier width

k_v = voltage dependent parameter

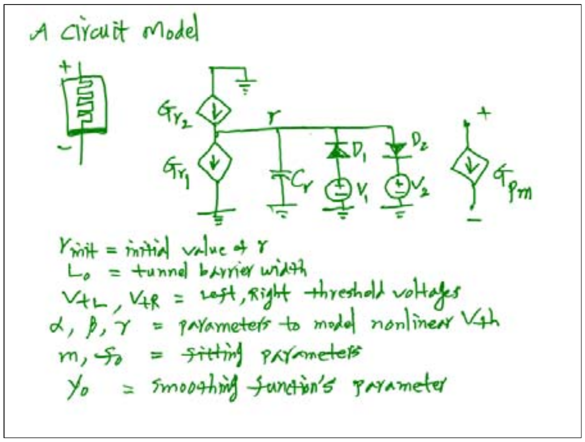


If L is expressed as a voltage dependent variable L_v

$R_t(L_v) = f_0 \frac{e^{2L_v}}{L_v}$

$L_v = L_0\left(1 - \frac{m}{r(v)}\right)$

$$\dot{r}(v) = \begin{cases} a_{reset} \frac{v + V_{reset}}{c + |v + V_{reset}|}, & -V_0 < V < V_{reset} \\ b v & V_{reset} < v < V_{set} \\ a_{set} \frac{v - V_{set}}{c + |v - V_{set}|} \end{cases}$$



A circuit Model

r_{init} = initial value of r

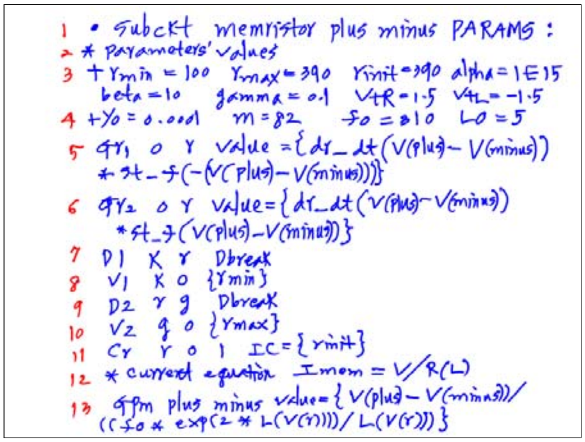
L_0 = tunnel barrier width

V_{tL}, V_{tR} = left, right threshold voltages

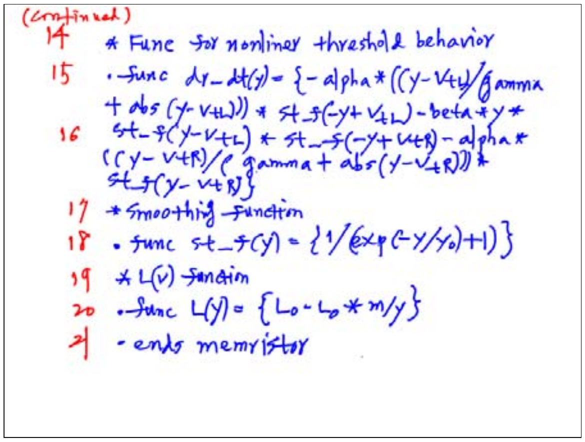
α, β, γ = parameters to model nonlinear V_{th}

m, f_0 = fitting parameters

y_0 = smoothing function's parameter

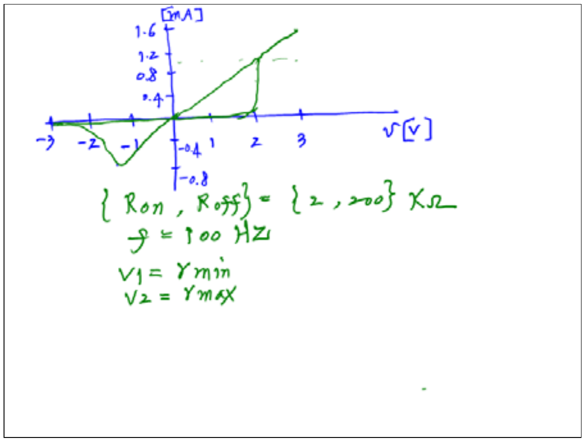


```
.subckt memristor plus minus PARAMS:
* parameters' values
+rmin = 100  rmax = 390  rinit = 390  alpha = 1E15
 beta = 10  gamma = 0.1  VtR = 1.5  VtL = -1.5
+y0 = 0.0001  m = 82  f0 = 810  L0 = 5
Gr1 0 r value = {dr_dt(V(plus) - V(minus))
 * st_f(-(V(plus) - V(minus)))}
Gr2 0 r value = {dr_dt(V(plus) - V(minus))
  * st_f(V(plus) - V(minus))}
D1 x r Dbreak
V1 x 0 {rmin}
D2 r g Dbreak
V2 g 0 {rmax}
Cr r 0 1 IC = {rinit}
* current equation Imem = V/R(L)
Gpm plus minus value = {V(plus) - V(minus))/
((f0 * exp(2 * L(V(r))))/L(V(r))}
```



(continued)

```
* Func for nonliner threshold behavior
.func dr_dt(y) = {-alpha*((y-VtL)/gamma
+ abs(y-VtL))) * st_f(-y+VtL) - beta*y*
st_f(y-VtL) * st_f(-y+VtR) - alpha*
((y-VtR)/(gamma + abs(y-VtR))) *
st_f(y-VtR)}
* Smoothing function
.func st_f(y) = {1/(exp(-y/y0)+1)}
* L(v) function
.func L(y) = {L0-L0*m/y}
.ends memristor
```

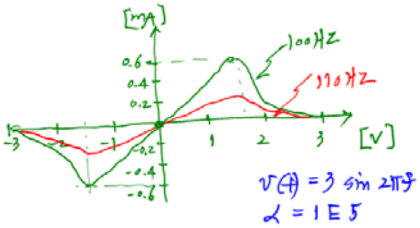


{Ron, Roff} = {2, 200} KΩ

f = 100 HZ

V1 = rmin

V2 = rmax



$v(t) = 3 \sin 2\pi f t$

$\alpha = 1E5$

HP's Model

$$v = M\left(\frac{w}{D}\right) i$$

D = the length of a thin oxide film

w = oxygen-deficient titanium oxide (tiO₂) width

$$M\left(\frac{w}{D}\right) = R_{off} - \Delta R \frac{w}{D}$$

memristance

$$\frac{dw}{dt} = \underset{\text{mobility of dopant}}{\mu} \frac{R_{on}}{D} \underbrace{f(w, i)}_{\text{window function}} i$$

$$f(w, i) = 1 - \left(\frac{2w}{D} - 1\right)^{2p}$$

p = a positive integer controlling the rate of decrease of the state variable as it approaches either boundary.

For example,

$p = 2$

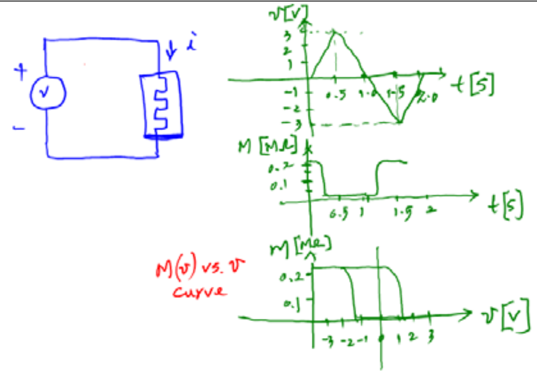
$D = 3\ nm$

$R_{off}/R_{on} = 10$

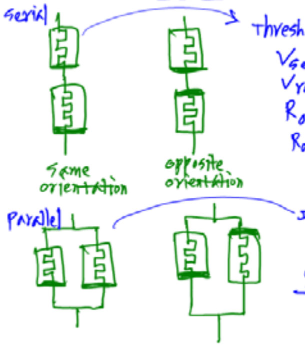
$\mu = 3 \times 10^{-8}\ m^2/V \cdot s$

$\{a_x, b, c, f_0, m, V_{set} = |V_{reset}|\}$

$= \{1000, 50, 0.1, 86.49, 50.06, 1.7[V]\}$



With SPICE or PSPICE simulations, various combinations of memristors have been studied.



Threshold voltage

$V_{set1} + V_{set2}$

$V_{reset1} + V_{reset2}$

$R_{on1} + R_{on2}$

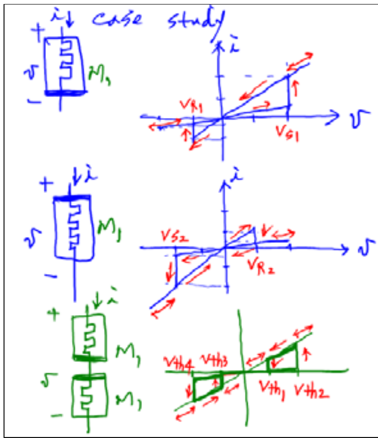
$R_{off1} + R_{off2}$

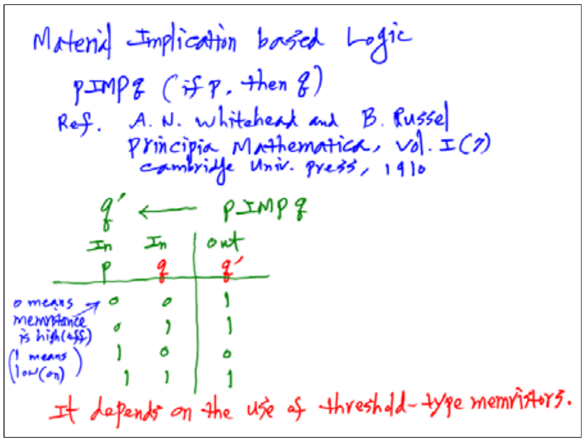
If identical ones,

Vset, Vreset same

$\frac{R_{on}}{2}, \frac{R_{off}}{2}$

case study





Material Implication based Logic

p IMP q (if p, then q)

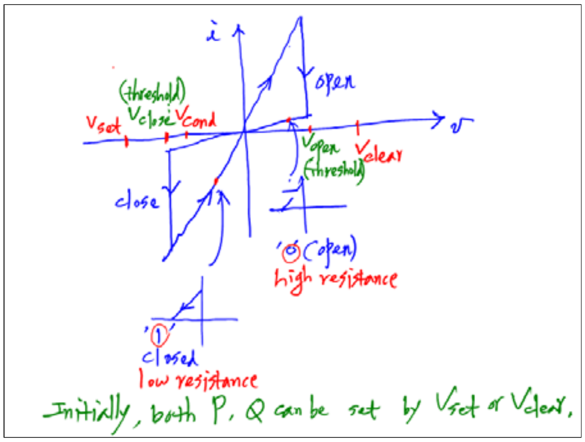
Ref. A. N. Whitehead and B. Russel
Principia Mathematica, Vol. I (?)
Cambridge Univ. Press, 1910

$q' \leftarrow p \text{ IMP } q$

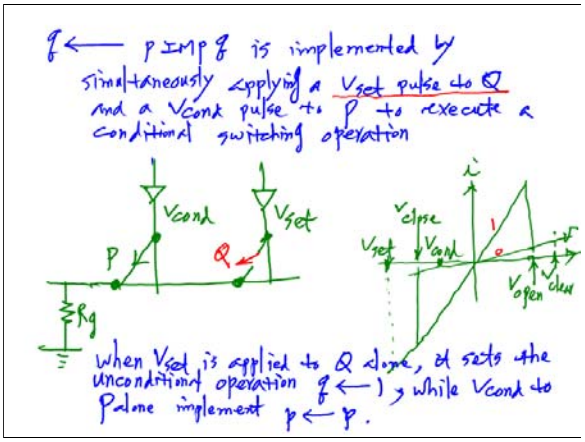
In p	In q	out q'
0	0	1
0	1	1
1	0	0
1	1	1

0 means memristance is high(off)
(1 means low(on))

It depends on the use of threshold-type memristors.

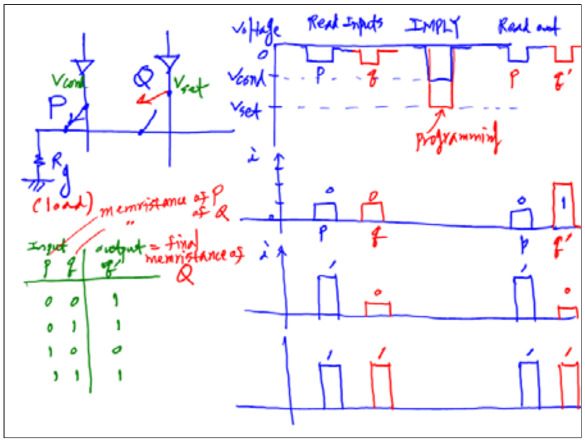


Initially, both P, Q can be set by V_{set} or V_{clear}.



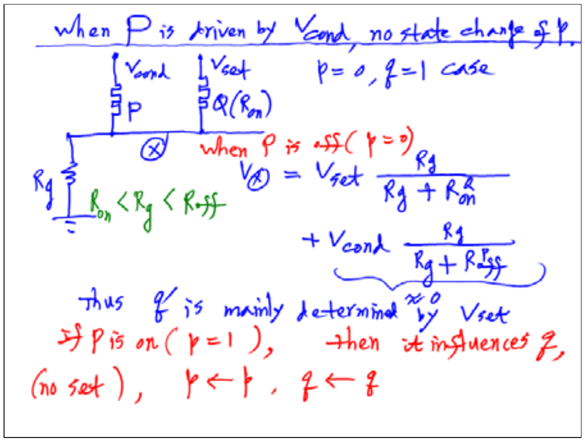
$q \leftarrow p \text{ IMP } q$ is implemented by simultaneously applying a V_{set} pulse to Q and a V_{cond} pulse to P to execute a conditional switching operation

When V_{set} is applied to Q alone, it sets the unconditional operation $q \leftarrow 1$, while V_{cond} to P alone implement $p \leftarrow p$.



Input p	q	output q'
0	0	1
0	1	1
1	0	0
1	1	1

output = final memristance of Q



When P is driven by V_{cond}, no state change of p.

$R_{on} < R_g < R_{off}$

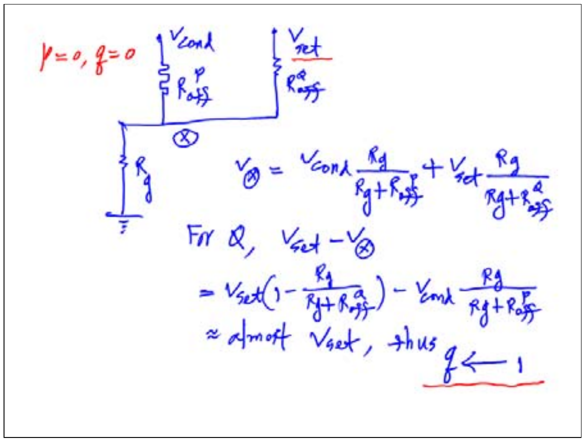
$p = 0, q = 1$ case

when P is off ($p = 0$)

$$V_{\otimes} = V_{set}\frac{R_g}{R_g + R_{on}^{Q}} + \underbrace{V_{cond}\frac{R_g}{R_g + R_{off}^{P}}}_{\approx 0}$$

thus q' is mainly determined by V_{set}

If P is on ($p = 1$), then it influences q, (no set), $p \leftarrow p$, $q \leftarrow q$



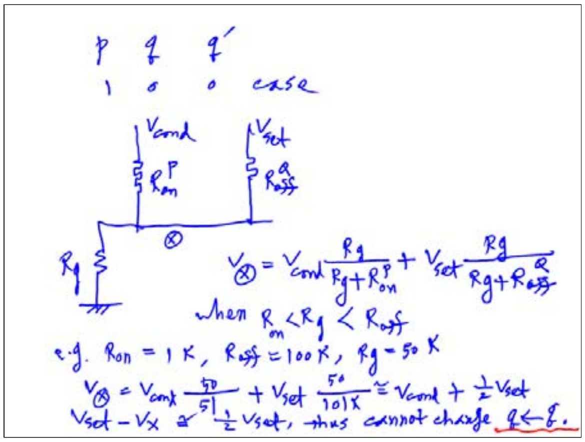
$p = 0, q = 0$

$$V_{\otimes} = V_{cond}\frac{R_g}{R_g + R_{off}^{P}} + V_{set}\frac{R_g}{R_g + R_{off}^{Q}}$$

For Q, $V_{set} - V_{\otimes}$

$$= V_{set}\left(1 - \frac{R_g}{R_g + R_{off}^{Q}}\right) - V_{cond}\frac{R_g}{R_g + R_{off}^{P}}$$

$\approx$ almost V_{set}, thus $q \leftarrow 1$



p q q'

1 0 0 case

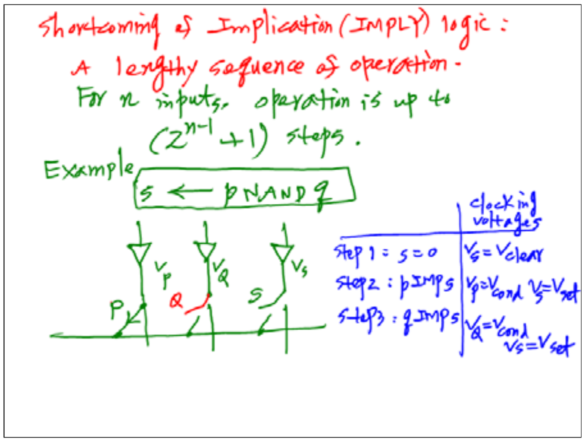
$$V_{\otimes} = V_{cond}\frac{R_g}{R_g+R_{on}^{p}} + V_{set}\frac{R_g}{R_g+R_{off}^{q}}$$

when $R_{on} < R_g < R_{off}$

e.g. $R_{on} = 1K$, $R_{off} = 100K$, $R_g = 50K$

$$V_{\otimes} = V_{cond}\frac{50}{51} + V_{set}\frac{50}{101K} \cong V_{cond} + \frac{1}{2}V_{set}$$

$V_{set} - V_x \approx \frac{1}{2}V_{set}$, thus cannot change $q \leftarrow q$.

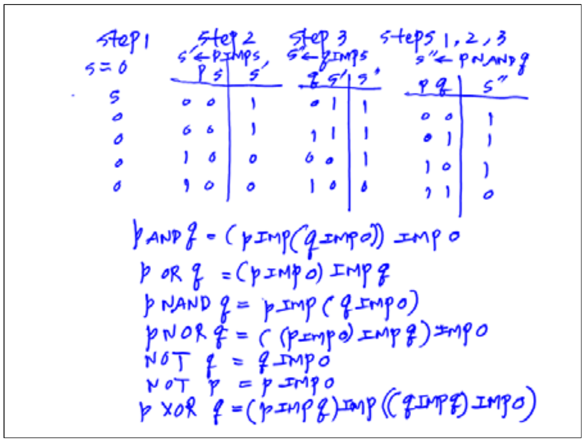

Shortcoming of Implication (IMPLY) logic:

A lengthy sequence of operation.

For n inputs, operation is up to $(2^{n-1}+1)$ steps.

Example $\boxed{s \leftarrow p \text{ NAND } q}$

	clocking voltages
step 1 : s = 0	$V_s = V_{clear}$
step 2 : p IMP s	$V_p = V_{cond}$ $V_s = V_{set}$
step 3 : q IMP s	$V_Q = V_{cond}$ $V_s = V_{set}$


step 1

s = 0

s
0
0
0
0

step 2

s' ← p IMP s,

p	s	s'
0	0	1
0	0	1
1	0	0
1	0	0

step 3

s'' ← q IMP s'

q	s'	s''
0	1	1
1	1	1
0	0	1
1	0	0

steps 1, 2, 3

s'' ← p NAND q

p	q	s''
0	0	1
0	1	1
1	0	1
1	1	0

p AND q = (p IMP (q IMP 0)) IMP 0

p OR q = (p IMP 0) IMP q

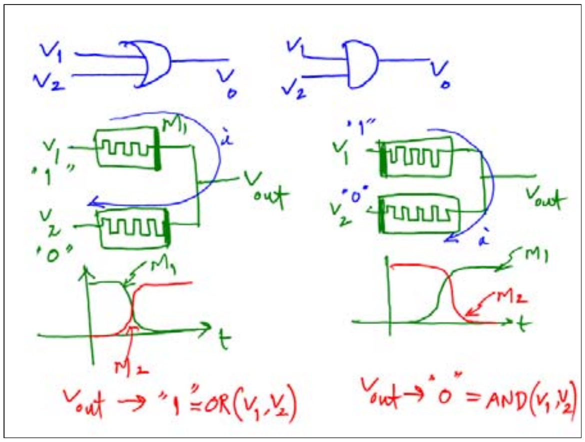
p NAND q = p IMP (q IMP 0)

p NOR q = ((p IMP 0) IMP q) IMP 0

NOT q = q IMP 0

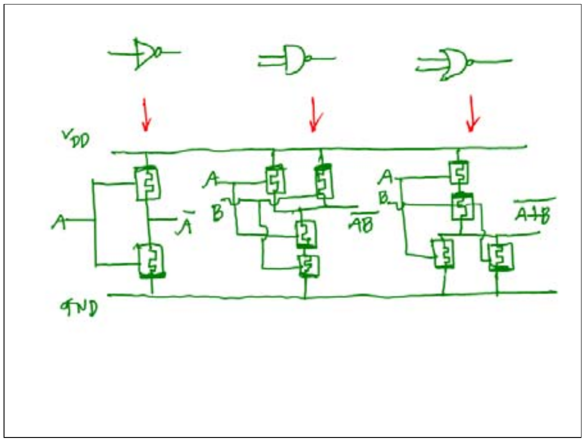
NOT p = p IMP 0

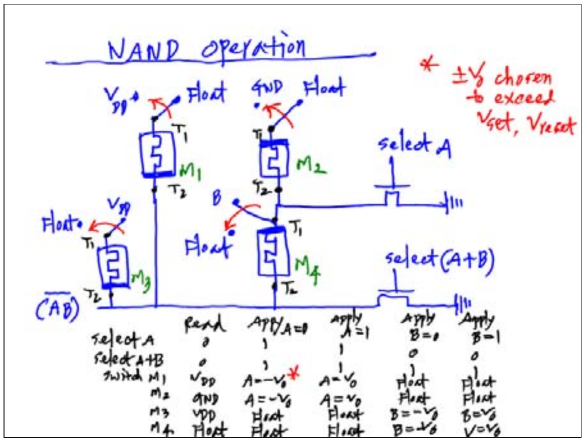
p XOR q = (p IMP q) IMP ((q IMP q) IMP 0)



$V_{out} \rightarrow$ "1" = OR(V_1, V_2)

$V_{out} \rightarrow$ "0" = AND(V_1, V_2)

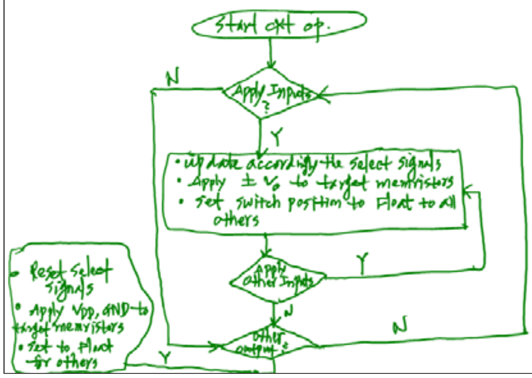



NAND operation

* ±V_0 chosen to exceed V_{set}, V_{reset}

	Read	Apply A=0	Apply A=1	Apply B=0	Apply B=1
select A	0	1	1	0	0
select A+B	0	1	1	1	1
switch M1	V_{DD}	$A=-V_0$ *	$A=V_0$	Float	Float
M2	GND	$A=-V_0$	$A=V_0$	Float	Float
M3	VDD	Float	Float	$B=-V_0$	$B=V_0$
M4	Float	Float	Float	$B=-V_0$	$V=V_0$

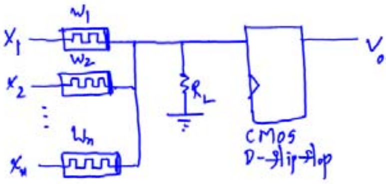
Operation Steps

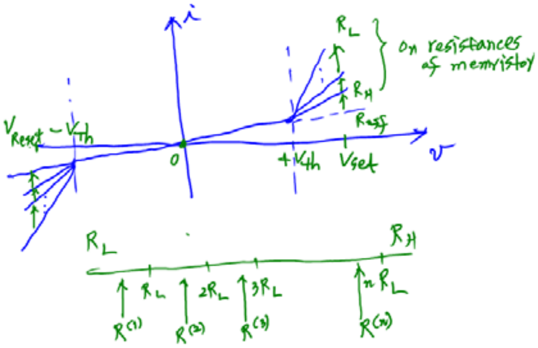


CMOS/Memristor Threshold Logic

n-input linear threshold logic (LTG)

$$f(x_1, x_2, \cdots, x_n) = \begin{cases} 1, & \text{if } \sum_{i=1}^{n} w_i x_i \geq X_{threshold} \\ 0, & \text{otherwise} \end{cases}$$





$w_i = \frac{1}{R^{(i)}}$, $(k-1)R_L < R^{(k)} < kR_L$

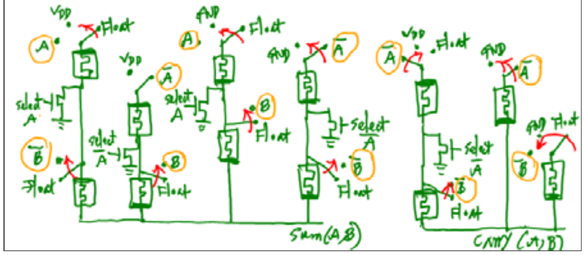
$n = R_H / R_L$

Half Adder

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Sum $(A,B) = XOR(A,B) = A\bar{B} + \bar{A}B$

Carry $(A,B) = AND(A,B) = AB$



Memristive Crossbar-Based Nonvolatile Memory

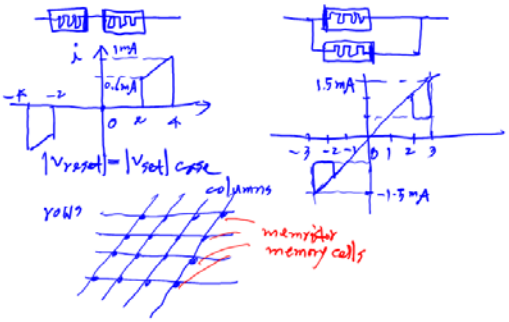
Advantage: scalability, density, CMOS compatibility, speed, energy efficiency, also radiation hardening.

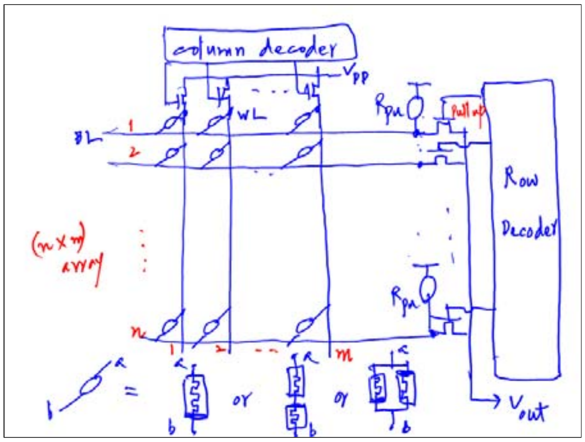
	DRAM	SRAM	Flash NAND	PCM	spin-transfer torque STT MRAM	ReRAM
Feature size	36-65nm	45nm	16nm	45nm	65nm	5nm
Cell area	6-30 F^2	140 F^2	4 F^2	4 F^2	20 F^2	4 F^2
Read time	2-10 ns	0.2ns	0.1 ms	12ns	35ns	<10ns
write time	2-10ns	0.2ns	0.1-1.0ms	100ns	35ns	<0.1ns
retention	4-64ms	N/A	>10yrs	>10yrs	>10yrs	>10yrs

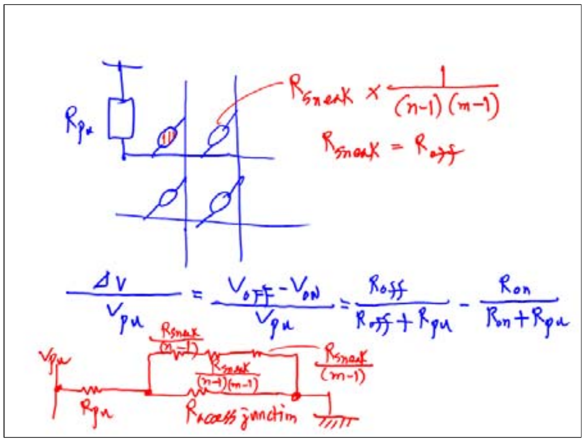
Redox-based RAM

(reduction-oxidation)

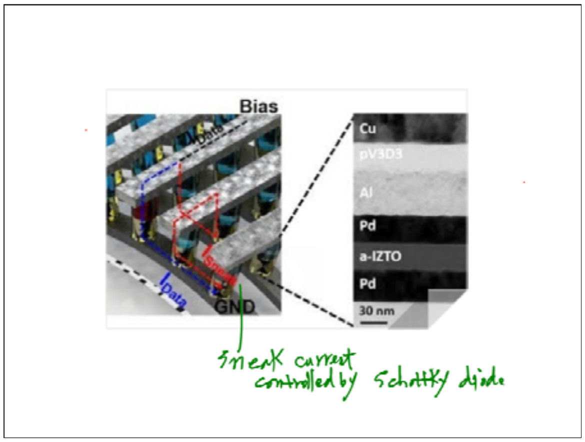
Anti-serial memristive switch (ASM)



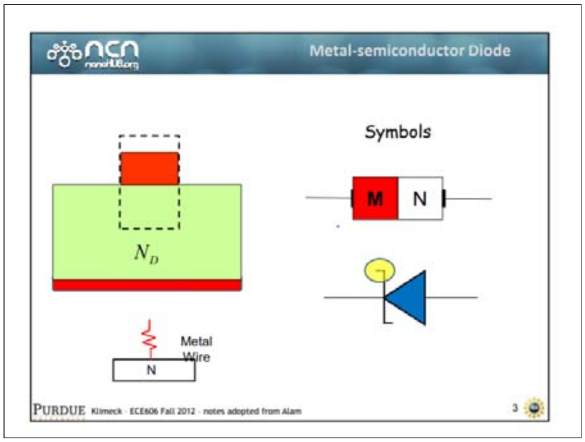




$$\frac{\Delta V}{V_{pu}} = \frac{V_{OFF} - V_{ON}}{V_{pu}} = \frac{R_{off}}{R_{off} + R_{pu}} - \frac{R_{on}}{R_{on} + R_{pu}}$$



sneak current controlled by Schottky diode



Metal-semiconductor Diode

PURDUE Klimeck - ECE606 Fall 2012 - notes adopted from Alam

3

- Metal-Semiconductor junction.
- Lower forward turn-on voltage.

No minority carrier storage!

- Steeper I-V curve
- Majority-carrier (Electron) device. Not like p-n diode using minority-carrier charge-storage effects.
- Higher cutoff frequency, reproducibility and ease of fabrication.
- Exitaxial and ion-implantation.
- Rectifying or non-rectifying (ohmic-contact)