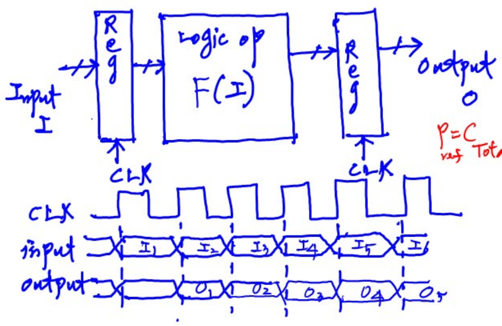
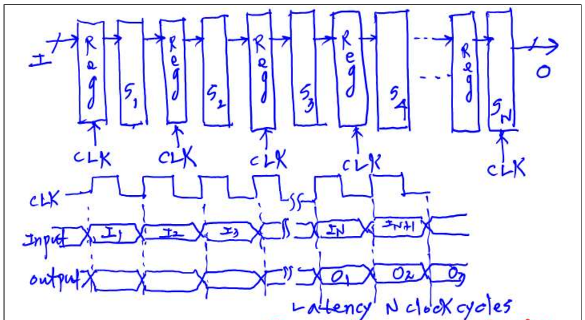
EE 222 W18 Lecture 12, Feb 22, 2018

Reducing Power through pipelining



$P_{ref} = C_{Total} V_{DD}^2 f_{CLK}$



$P_{pipeline} = (C_{Total} + (N-1) C_{Reg}) V_{DDL}^2 f_{CLK}$

$$\frac{P_{pipeline}}{P_{ref}} = \frac{C_{Total} + (N-1) C_{Reg}}{C_{Total}} \left(\frac{V_{DDL}}{V_{DD}}\right)^2 = \left(1 + (N-1)\frac{C_{Reg}}{C_{Total}}\right)(V_{DDL}/V_{DD})^2$$

Example

C_{Total} C_{Reg}	V_{DD}	V_T	V_{DDL}	V_T	f_{CLK}
$\frac{C_{Reg}}{C_{Total}} \simeq 0.1$	5V	0.8V	2	0.8	20MHz

can lower V_{DD} for S_K to compute in $T = \frac{1}{f_{CLK}}$

$$\left(1 + (N-1)\frac{C_{Reg}}{C_{Total}}\right)\left(\frac{2}{5}\right)^2 = 1.0 \times (0.4)^2 = 0.16$$

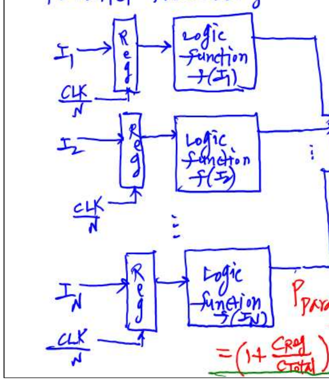
$\frac{C_{Reg}}{C_{Total}} \approx 0$ 84% saving

$N = 8$

$$\left[1 + 7(0.1)\right](0.4)^2 = 1.7 \times 0.16 \cong 0.3$$

70% saving

Parallel Processing

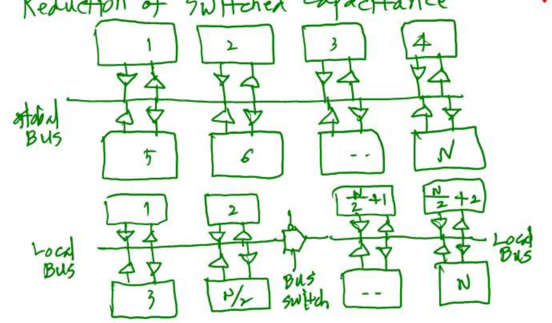


$$P_{parallel} = N C_{Total} V_{DD//}^2 \frac{f_{CLK}}{N} + C_{Reg} V_{DD//}^2 f_{CLK} = \left(1 + \frac{C_{Reg}}{C_{Total}}\right) C_{Total} \cdot V_{DD//}^2 f_{CLK}$$

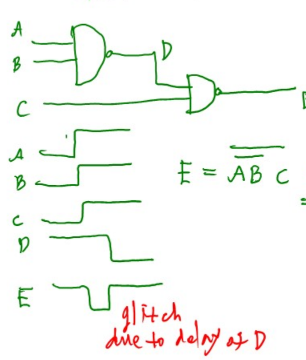
$$\frac{P_{parallel}}{P_{ref.}} = \left(1 + \frac{C_{Reg}}{C_{Total}}\right)\left(\frac{V_{DD//}}{V_{DD}}\right)^2$$

O(x) saving

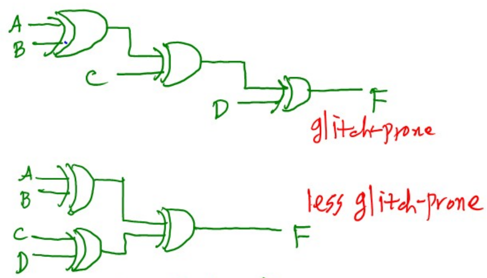
Reduction of Switched Capacitance



"glitch" Reduction



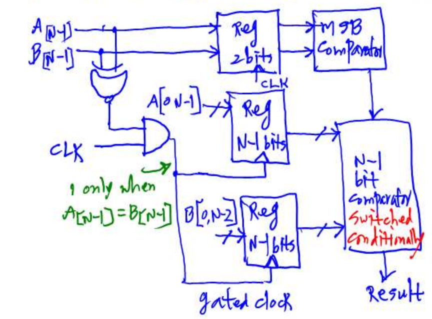
$$E = \overline{\overline{AB}\,C} = \overline{\overline{AB}} + \overline{C} = AB + \overline{C}$$



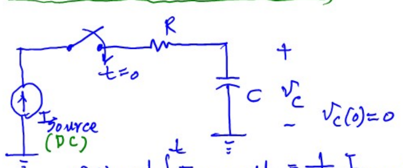
$(A \oplus B) \oplus (C \oplus B) = F$

Gated clocking

example N-bit number comparator



Adiabetic Circuits



$v_C(t) = \frac{1}{C}\int_0^t I_{source}\,dt = \frac{1}{C} I_{source}\, t$

$I_{source} = C\,\frac{v_C(t)}{t}$ (1)

$E_{dissipation}(t) = R\int_0^t I_{source}^2\,dt = R\, I_{source}^2\, t$ (2)

$E_{dissipation}(T) = R\left(\frac{C v_C(t)}{t}\right)^2 t \Big|_{t=T} = \frac{RC}{t}\, C v_C^2(t)\Big|_{t=T}$

From (1), $I_{source} = C\,\frac{v_C(t)}{t}$

Energy stored in the capacitor

$E_C(t) = \frac{1}{2} C v_C^2(t)$

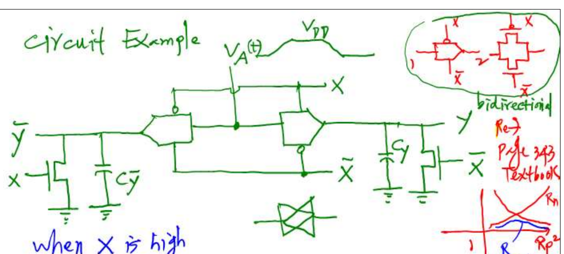
Energy Dissipated in R is

$E_{dissip} = \frac{RC}{t}\, C\, v_C^2(t)$

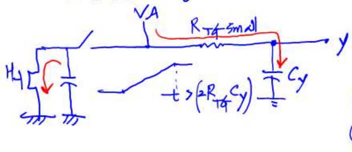
For $t > 2RC$ $\quad E_{dissip} < E_C$

when the constant current source is used to "slowly" charge up the capacitor, dissipated energy can be made smaller ($< E_C$). If the source current direction is reversed, then the energy stored in the capacitor less E_{dissip} can be returned! The slower the time, the more can be returned.

Circuit Example



when X is high



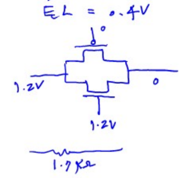
$E_C = \frac{1}{2} C_y\, y^2(t)$ stored

$E_{dissip}\ \frac{R_{TG} C_y}{t}\, C_y y^2(t)$

(For $t > 2R_{TG} C_y$, $E_{dissip} < E_C$)

Example

	NMOS	PMOS
V_T =	0.53 V	−0.51 V
k' =	98 μA/V²	46 μA/V²
L =	10 nm	10 nm
EL =	0.4 V	1.8 V



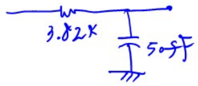
$I_{DS_N}^{sat} \cong k'\frac{W}{L}\left[\frac{(1.2-0.53)^2}{2}\right] \cong 980\,\mu A/V^2\, \frac{(0.45)}{2} V^2 \cong 0.22\,mA$ (if $W/L = 10$)

$I_{DS_p} \cong 460\,\mu A/V^2\, \frac{(1.2-0.51)^2}{2}\,[V]^2 = 0.11\,mA$

$R_N = \frac{1.2\,V}{0.22\,mA} = 5.45\,k\Omega$

$R_p = \frac{1.2\,V}{0.11\,mA} = 10.9\,k\Omega$

$R_{TG} = R_N \| R_p = \frac{5.45 \times 10.9}{5.45 + 10.9} = 3.82\,k\Omega$

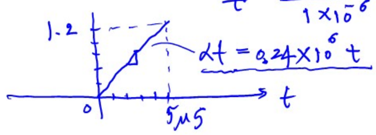


$RC = 3.82\times10^{3} \times 50\times10^{-15} = 191$ ps

If $t = 5RC$, then $t = 0.955$ ns

$t = 50RC$, $t = 50 \times 191$ ps $= 9.55$ ns

$t = 1\mu s$, $\frac{RC}{t} = \frac{191\times10^{-12}}{1\times10^{-6}} = 191\times10^{-6} \approx 0$



$C_y \frac{dy}{dt} = \frac{V_A - y}{R_{T4}}$

$(R_{T4}C_y)\frac{dy}{dt} + y = V_A = \alpha t$, $t \geq 0$ — α is small (slowly rising V_A)

$\downarrow \mathcal{L}$

$(R_{T4}C_y s + 1)Y(s) = \frac{\alpha}{s^2}$

$Y(s) = \frac{\alpha}{s^2(R_{T4}C_y s+1)} = \frac{-R_{T4}C_y\alpha}{s} + \frac{\alpha}{s^2} + \frac{(R_{T4}C_y)^2\alpha}{R_{T4}C_y s+1}$

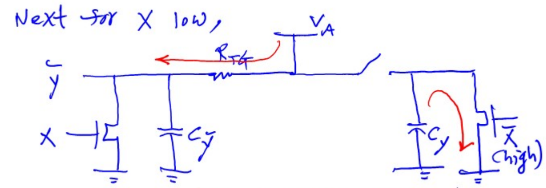
$y(t) = -\alpha R_{T4}C_y + \alpha t + \alpha (R_{T4}C_y)^2 e^{-\frac{1}{R_{T4}C_y}t}$

For large t, small α, small $R_{T4}C_y$,

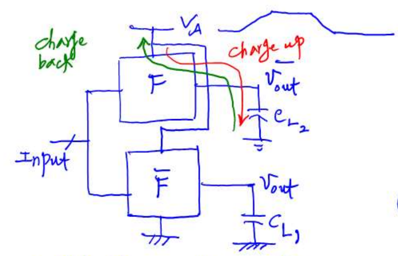
$y(t) = \alpha t \ (= V_A)\big|_{t=T}$ charge up to V_A level

then the E_C energy can be retried to power supply side.
Or the $y(t)$ can be used to drive other gates w/o V_A.

Next for X low,



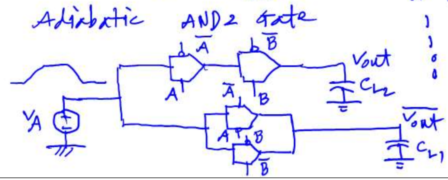
Same analysis for $\bar{y}(t)$ with
V_A supply (now using the energy retrieved)
Thus, adiabatic logic with energy cycling.



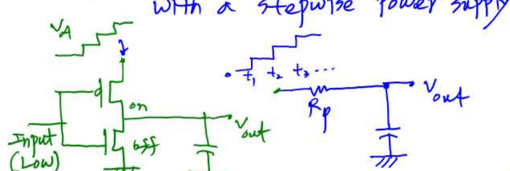
(C_{L_1}, C_{L_2} reset to 0)

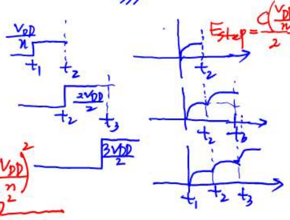
A	B	V_{out}	$\bar{V}_{out}$
1	1	V_A	0
1	0	0	V_A
0	1	0	V_A
0	0	0	V_A

Adiabatic AND2 Gate



Analysis of a CMOS Inverter
with a Stepwise Power supply.





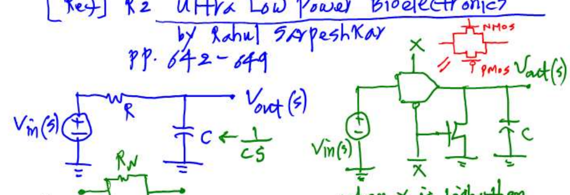
$E_{step} = \frac{C\left(\frac{V_{DD}}{n}\right)^2}{2}$

After n steps

$E_C = n\, E_{step} = n\, \frac{1}{2} C \left(\frac{V_{DD}}{n}\right)^2 = \frac{1}{2n} C V_{DD}^2$

A More generalized analysis of
adiabatic circuits

[Ref] R2 Ultra Low Power Bioelectronics
by Rahul Sarpeshkar
pp. 642–649



when X is high then the rest circuit model.

$V_{out}(s) = V_{in}(s)\, \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}}$

$= V_{in}(s)\, \frac{1}{1 + RCs}$, $I_R(s) = \frac{V_{in}(s) - V_{out}(s)}{R}$

$$\Rightarrow I_R(s) = V_{in}(s)\,\frac{Cs}{1+RCs}$$

power dissipated in R

$$P_R(s) = |I_R(s)|^2 R$$

$$P_R(j\omega) = |I_R(j\omega)|^2 R$$

$$= |V_{in}(j\omega)|^2 \left|\frac{j\omega C}{1+j\omega RC}\right|^2 R$$

$$= \frac{|V_{in}(j\omega)|^2}{R}\,\frac{\omega^2(RC)^2}{1+\omega^2(RC)^2}$$

Energy $= \int_0^T P_R(t)\,dt$, where $\omega T = 2\pi$ + $T = \frac{2\pi}{\omega}$

$$E_R(j\omega) = P_R(j\omega)\,T = \underline{\frac{|V_{in}(j\omega)|^2}{R}\,\frac{\omega^2(RC)^2}{1+\omega^2(RC)^2}\,\frac{2\pi}{\omega}}$$

$$E_R(j\omega) = \frac{|V_{in}(j\omega)|^2}{R}\,\frac{\omega^2(RC)^2}{1+\omega^2(RC)^2}\,\frac{2\pi}{\omega}$$

$$E_C(j\omega) = \frac{1}{2}C\,|V_{out}(j\omega)|^2 \underset{\substack{\text{when}\\ V_o = V_{in}}}{\uparrow} \frac{1}{2}C\,|V_{in}(j\omega)|^2$$

$$\frac{E_R(j\omega)}{E_C(j\omega)} = \frac{\frac{\cancel{|V_{in}(j\omega)|^2}}{R}\,\frac{\omega^2(RC)^2}{1+\omega^2(RC)^2}\,\frac{2\pi}{\omega}}{\frac{1}{2}C\,\cancel{|V_{in}(j\omega)|^2}}$$

$$= \frac{4\pi\,\omega^2(RC)^2}{\omega RC\,(1+\omega^2(RC)^2)}$$

$$= \frac{4\pi\,\omega RC}{1+(\omega RC)^2} \underset{\substack{\text{when}\\ (\omega RC<1)}}{\uparrow} 4\pi\,\frac{1}{\left(\frac{1}{\omega RC}\right)} = \frac{4\pi}{Q}$$

$\boxed{Q = \frac{1}{\omega RC}}$ quality ~~factor~~

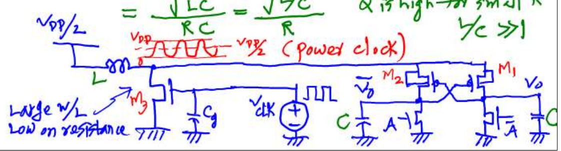
$Q = \frac{1}{\omega RC}$ is high when ωRC is small ($\frac{E_R}{E_C}$ is made small)

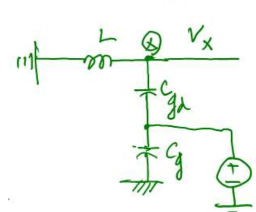
To make Q high, make $\omega RC = \frac{2\pi}{T} RC = 2\pi\frac{RC}{T}$ small by making $\boxed{T \gg RC}$.

Adiabatic clock

$Q = \frac{1}{\omega_0 RC}$ $\quad \omega_0$ (resonance freq) $= \frac{1}{\sqrt{LC}}$

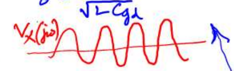
$= \frac{\sqrt{LC}}{RC} = \frac{\sqrt{L/C}}{R}$ $\quad$ Q is high for small R, $L/C \gg 1$





$$V_X(j\omega) = \frac{j\,\omega/\omega_0^2}{j\,\omega/\omega_0^2 + 1}\,V_{CLK}(j\omega)$$

$$\omega_0 = \frac{1}{\sqrt{LC_{gd}}}$$

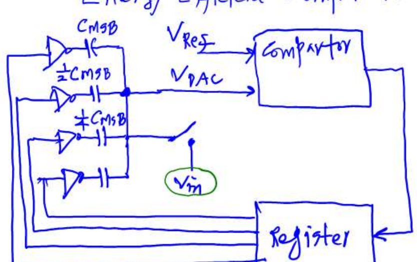


At ⓧ $\quad \frac{V_X(s)}{Ls} = \frac{V_{CLK}(s) - V_X(s)}{\left(\frac{1}{C_{gd}s}\right)} = 0$

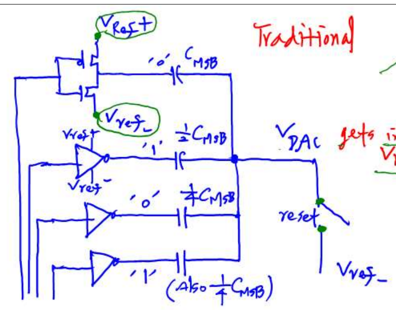
$$V_X(s)\left[C_{gd}s + \frac{1}{Ls}\right] = s\,V_{CLK}(s)\,C_{gd}$$

$$V_X(s) = \frac{C_{gd}s}{C_{gd}s + \frac{1}{Ls}}\,V_{CLK}(s) = \left[\frac{LC_{gd}s}{LC_{gd}s+1}\right]V_{CLK}(s)$$

Energy Efficient Comparator in ADC



Adiabetic charging for 3 MSBs only since for lower bits savings are < 2X.



Traditional

V_{DAC} gets initialized to V_{ref-}

from register

Reset switch initializes V_{DAC} to $V_{ref-} \pm \sqrt{\frac{kT}{C_{Total}}}$

$C_{Total} = 2C_{MSB} + C_{parasitic}$, T = temperature [°F]

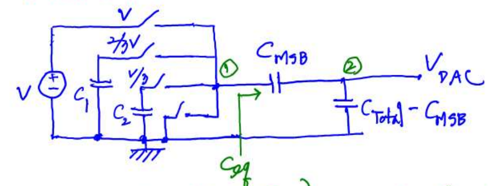
$$V_{DAC}(C_{Total}) = C_{MSB}\cdot 0 + \frac{1}{2}C_{MSB}('0'-'1')$$
$$+ \frac{1}{4}C_{MSB}\cdot 0 + \frac{1}{4}C_{MSB}('0'-'1')$$
$$= C_{MSB}\left(1+\frac{1}{4}\right)\cdot 0 + \frac{3}{4}C_{MSB}('0'-'1')$$

$'0'-'1' = V_{ref-} - V_{ref+} = -\Delta V$ (resolution)

Say $\Delta V = \frac{1}{3}V$

$$V_{DAC} = \frac{-\frac{3}{4}C_{MSB}\left(\frac{1}{3}V\right)}{C_{Total}} = -\frac{1}{4}\frac{C_{MSB}}{2C_{MSB}+C_{par.}}V$$
$$\simeq -\frac{1}{8}V$$

Alternative scheme



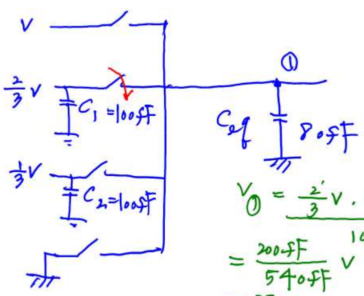
$$C_{eq} = \frac{C_{MSB}(C_{Total}-C_{MSB})}{C_{MSB}+(C_{Total}-C_{MSB})} = C_{MSB}\left(1-\frac{C_{MSB}}{C_{Total}}\right)$$

Switching energy is reduced by ×3 (with $n=3$ levels of V used)

e.g.) $V = 1V$
$C_{Total} = 500fF$

If $C_{MSB} = 100fF$

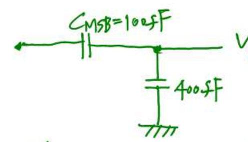
$$C_{eq} = 100fF\left(1-\frac{100fF}{500fF}\right) = 80fF$$



assume to be zero

$$V_{①} = \frac{\frac{2}{3}V\cdot 100fF + V_{①}(0)\,80fF}{100fF+80fF}$$
$$= \frac{200fF}{540fF}V$$
$$= 0.37V$$

0.37 V



$$V_{DAC} = 0.37V\ \frac{100}{100+400} = 0.074V$$

$$\left(0.37\ \frac{\frac{1}{400}}{\frac{1}{100}+\frac{1}{400}}\right)$$