EE 222 Lecture 3 Jan 16, 2018

HW2 Prob. 3.1, Prob. 3-6 & Prob 3.14
HW3 Prob 4.1, Prob. 4.3

Help for CAD tools, HW solutions

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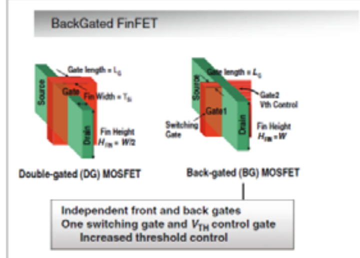
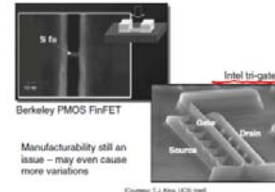
FINFETs



Slide 2.46
This increased two-dimensional control can be exploited in a number of ways. In the dual-gated device, the fact that the gate is controlling the channel from both sides (as well as the top) leads to increased process transconductance. Another option is to remove the top part of the gate, leading to the back-gated transistor. In this structure, one of the gates acts as the standard control gate, whereas the other is used to manipulate the threshold voltage. In a sense, this device offers similar functionality as the buried-gate FD-SOI transistor discussed earlier. Controlling the work functions of the two gates through the selection of appropriate type and quantity of the dopants helps to maximize the range and sensitivity of the control knobs.

New Transistors: FinFETs



Berkeley PMOS FinFET

Manufacturability still an issue – may even cause more variations

(Courtesy: T.J. King, UCB; Intel)

Slide 2.47
The fact that the FinFET and its cousins are dramatically different devices compared to your standard bulk MOS transistor is best-illustrated with these pictures from Berkeley and Intel. The process steps that set and control the physical dimensions are entirely different. Although this creates new opportunities, it also brings challenges, as the process steps involved are vastly different. The ultimate success of the FinFET depends greatly upon how these changes can be translated into a scalable, low-cost and high-yield process – some formidable question, indeed! Also unclear at this time is how the adoption of such a different structure impacts variability, as critical dimensions and device parameters are dependent upon entirely different process steps.

An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications

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EPFL - EKV Model (1995)

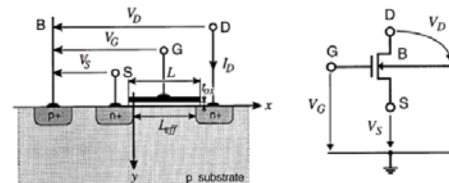


Fig. 1. Cross-section of an idealized n-channel MOS transistor and the corresponding symbol. All voltages are referred to the local p-type substrate.

Table 1. Definitions used in the model.

Symbols	Description	Units
q	Elementary charge	$A \cdot s$
$U_T = (k \cdot T)/q$	Thermodynamic voltage	V
n_i	Intrinsic carrier concentration of Si	m^{-3}
$\varepsilon_s, \varepsilon_{ox}$	Dielectric constant of Si and SiO_2	F/m
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	Gate oxide capacitance per unit area	F/m^2
N_{sub}	Doping concentration of substrate	m^{-3}
$\Phi_F = U_T \cdot ln(N_{sub}/n_i)$	Fermi potential in the substrate	V
V_{FB}	Flat-band voltage	V
$\Psi, \Psi_s = \Psi(y = 0)$	Electrostatic potential and surface potential	V
$V_{ch} = \phi_n - \phi_p = \phi_n - \Phi_F$	Channel potential	V
Q'_{inv}	Mobile inversion charge per unit area	$(A \cdot s)/m^2$
μ_n	Mobility of electrons in the channel	$m^2/(V \cdot s)$

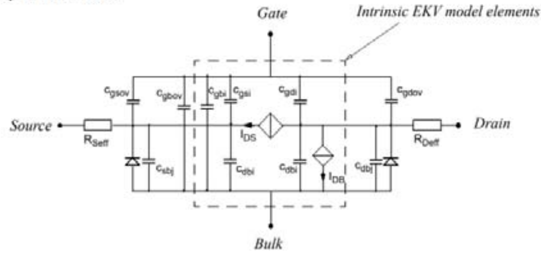
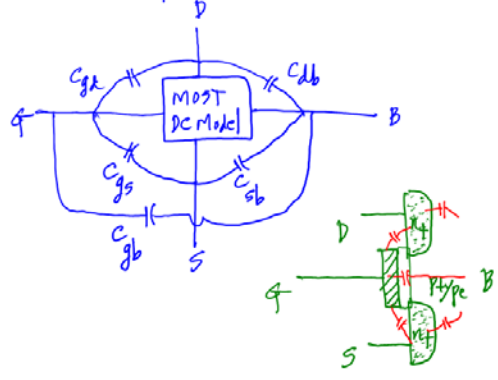
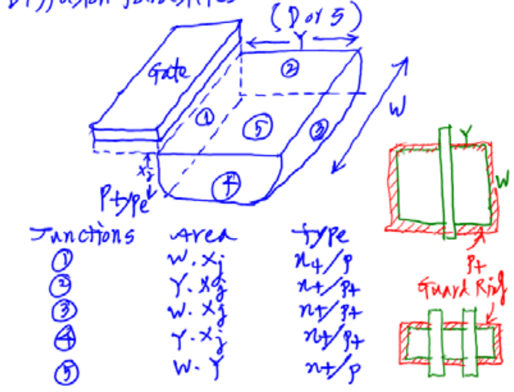


Table 2. Drain current in strong and in weak inversion.

Mode	Weak Inversion	Strong Inversion
Conduction	$K_w \cdot \beta \cdot U_T^2 \cdot e^{V_P/U_T} \cdot \left[e^{-V_S/U_T} - e^{V_D/UT}\right]$ for: $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_S \cong V_D \end{cases}$	$n \cdot \beta \cdot \left[V_P - \frac{V_S+V_D}{2}\right] \cdot (V_D - V_S)$ for: $\begin{cases} V_S \le V_P \\ V_D \le V_P \end{cases}$
Forward Saturation	$K_w \cdot \beta \cdot U_T^2 \cdot e^{\frac{V_P - V_S}{U_T}}$ for: $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_D - V_S \gg U_T \end{cases}$	$\frac{n \cdot \beta}{2} \cdot (V_P - V_S)^2$ for: $\begin{cases} V_S \le V_P \\ V_D > V_P \end{cases}$
Blocked	0 for: $\begin{cases} V_S \gg V_P \\ V_D \gg V_P \end{cases}$ or $V_S = V_D$	0 for: $\begin{cases} V_S > V_P \\ V_D > V_P \end{cases}$

U_T defined in Table 1





n+ | p

x_d (depletion distance)

$$x_d = \sqrt{\frac{2\epsilon_{si}}{q}\,\frac{N_A+N_D}{N_A N_D}\,(\phi_0 - V)}$$

$$\phi_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

where $n_i = 1.45\times 10^{10}/cm^2$

$$Q_j \doteq A\,q\,\frac{N_A N_D}{N_A+N_D}\,x_d$$

$$= A\sqrt{2\epsilon_{si}\,q\,\frac{N_A N_D}{N_A+N_D}\,(\phi_0 - V)}$$

$$C_j = \left|\frac{dQ_j}{dV}\right| = A\sqrt{\frac{\epsilon_{si}\,q}{2}\left(\frac{N_A N_D}{N_A+N_D}\right)\frac{1}{\phi_0 - V}}$$

$$= \frac{A\,C_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}, \quad m = \frac{1}{3} \sim \frac{1}{2}$$

Example For $N_A = 1.6\times 10^{18}/cm^3$

$N_D = 2.2\times 10^{18}/cm^3$

$n_i = 1.45\times 10^{10}/cm^3$

$$\phi_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2} = 26mV\,\ln\frac{1.6\times 10^{18}\cdot 2.2\times 10^{18}}{(1.45\times 10^{10})^2}$$

$$= 0.97\,[V]$$

$$C_{j0} = \sqrt{\frac{\epsilon_{si}\,q}{2}\,\frac{N_A N_D}{N_A+N_D}\,\frac{1}{\phi_0}}$$

$$\simeq \sqrt{\frac{11.7\times 8.854\times 10^{-14}\,F/cm\cdot 1.6\times 10^{-19}C}{2}\left(\frac{1.6\times 10^{18}\cdot 2.2\times 10^{18}}{1.6\times 10^{18}+2.2\times 10^{18}}\right)\frac{1}{0.97V}}$$

$$= 2.81\times 10^{-2}\,[F/cm^2]$$

$$C_{eq} = A\,C_{j0}\,K_{eq}, \quad K_{eq} = \frac{2\sqrt{\phi_0}}{V_2 - V_1}\left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1}\right)$$

For $V_1 = 0V$, $V_2 = -1V$, $K_{eq} = \frac{2\sqrt{0.97}}{-1}\left(\sqrt{0.97-(-1)} - \sqrt{0.97}\right) = 0.82$

For $A = 100\,\mu m^2$, $C_{eq} = (100\times 10^{-8}\,cm^2)(2.81\times 10^{-2}\,F/cm^2)(0.82) = 230\,fF$

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EECS Department
University of California, Berkeley
Technical Report No. UCB/ERL M98/51
1998

http://www2.eecs.berkeley.edu/Pubs/TechRpts/1998/ERL-98-51.pdf

BSIM3v3 is the latest industry-standard MOSFET model for deep-submicron digital and analog circuit designs from the BSIM Group at the University of California at Berkeley. BSIM3v3.2 is based on its predecessor, BSIM3v3.1. Its many improvements and enhancements include

* A new intrinsic capacitance model (the Charge Thickness Model), considering the finite charge layer thickness determined by quantum effect, is introduced as capMod 3 It is very accurate in all operating regions.

* Modeling of C-V characteristics at the weak-to-inversion transition is improved.

* The T(ox) dependence is added into the threshold voltage model.

* The flat-band voltage is added as a new model parameter to accurately model MOSFET's with different gate materials.

* Substrate current dependence on the channel length is improved.

* The non-quasi-static (NQS) model is restructured to improve the model accuracy and simulation efficiency. NQS is added in the pole-zero analysis.

* The temperature dependence is added to the diode junction capacitance model.

* The DC junction diode model now supports a resistance-free diode model and a current-limiting feature.

* Option of using C-V inversion charge equations of capMod 0, 1, 2 or 3 to calculate the thermal noise when noiMod == 2 or 4 is added.

* The small negative capacitance of C(gs) and C(gd) in the accumulation-depletion regions is eliminated.

* A separate set of length/width-dependence parameters is introduced in the C-V model to better fit the capacitance data.

* Parameter checking is added to avoid bad values for certain parameters.

* Known bugs are fixed.

Meticulous care has been taken to accomplish the above model enhancements with high levels of accuracy and fast SPICE convergence properties. In addition, every effort has been made to maintain the backward compatibility with the previous version except for the following change:

Softwares for Circuit Simulation:

1. OrCAD Pspice :
   http://www.orcad.com/resources/download-orcad-lite

2. Tools by Linear Technology(now part of Analog Devices):
   http://www.linear.com/designtools/software/

Layout tools:

1. Magic VLSI Layout Tool:
   http://opencircuitdesign.com/magic/index.html

2. Cadence Virtuoso:
   https://vlsiwiki.soe.ucsc.edu/index.php/Technology_Setup

   Note: you will have to remotely login to the server using this command:
   ssh -Y waterdance.soe.ucsc.edu and type in your bluepassword.
   If that doesn't work, please contact the ITS Department or contact Eric Shell: Baskin Engineering, Room 313, eshell@ucsc.edu

You can also access cadence in the baskin engineering lab 105.(The computers in that lab run on unix os)