EE 222 Lecture 6 Jan 5, 2017

RC delay analysis [Text 17-24]

\[ V_x(t) = \int_{-\infty}^{t} v(t) \, \text{d}t \]

\[ H(t) = \frac{e^{-t/\tau}}{1 + RC} \]

\[ V_{in}(t) = H(t) \cdot v_{in}(t) = \frac{1}{1 + RC} \cdot \frac{1}{1 + RC} \]

\[ V_x(t) = H(t) \cdot v_{in}(t) = \frac{e^{-t/\tau}}{1 + RC} \cdot \frac{1}{1 + RC} \]

When \( t = \tau \), \( v_x(\tau) = 1 - e^{-1} \)

In this case, there is no time constant corresponding to \( \tau \), hence \( v_x(\tau) \) is almost 1.

Next consider the following circuit:

\[ V_{in} \]

Let \( N \) be the total number of nodes and \( C \) be the total number of capacitors. The unique path from input to node \( i \)

\[ P_j = 0 \quad \text{if node} \quad j \quad \text{is not connected to the input} \]

\[ P_j = 1 \quad \text{if node} \quad j \quad \text{is connected to the input} \]

\[ P_{ij} = \text{the common portion of} \quad P_i \quad \text{and} \quad P_j \]

\[ P_i = \bigoplus_j P_{ij} \]

\[ P_{ij} = \sum_j C_j \sum_k R_k \quad \text{Re} \quad P_{ij} \quad P_k \]

Example: \( D_7 = \sum_{j=1}^{N} C_j \sum_k R_k \quad P_{ij} \quad P_j \quad P_k \quad P_{ij} \quad P_k \)

\[ = C_1 + C_2 + C_3 + C_4 \quad + C_5 \quad (R_1 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8) \]

\[ + C_9 \quad (R_1 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8) \]

Conclusion: \( D_7 \) is the sum of all possible combinations of resistance and capacitance.

\[ D_{max} \text{ value: } 6.5 \text{ mm} \]

Technology case:

\[ L = 3 \mu m \quad W = 2.5 \mu m \quad P_{ly} = 1 \mu m \]

Metal 1 thickness = 1.8 \mu m

Minimum width = 0.4 \mu m

Metal 1 max yield area (A) = 0.2 \mu m

\[ R_{min} = 1.8 \times 10^{-6} \Omega \quad \text{A} \text{mm}^{-2} \]

\[ = 1.8 \times 10^{-6} \quad \text{A} \text{mm}^{-2} \]

For \( L = 9 \mu m, \quad W = 5 \mu m \)

\[ R_{on} = \frac{1}{2} \times 10^{-6} \Omega \quad \text{mm}^{-2} \]

\[ C_{on} = 0.02 \times 10^{-6} \text{ F} \quad \text{mm}^{-2} \times 2 \times \text{mm} \]

\[ C_{on} = 0.02 \times 10^{-6} \text{ F} \quad \text{mm}^{-2} \times 2 \times \text{mm} \]

\[ R_{off} = 900 \Omega \quad \text{mm}^{-2} \]

Different models:

- L model
- Π model
- T model
Power Meter (Ref. Text section 6.7) by S. Kanji

\[ \text{Power} = \frac{1}{2} \int_0^T \dot{V}(t) \ddot{V}(t) \, dt = \left[ \frac{1}{2} \int_0^T \ddot{V}(t) \, dt \right] V_p \]

Example

\[ \text{VDD} = 3.3 \text{V} \]
\[ \text{T}_{\text{CC}} = 55 \text{C} \]
\[ R_{\text{L}} = 5 \Omega \]
\[ C_{\text{L}} = 1 \text{nF} \]

\[ \text{Power} = C_{\text{L}} \text{VDD}^2 = 2 \times \text{VDD} \times 3.3 \text{V} \]

\[ \text{Energy-Delay Product (EDP)} \]
\[ \text{EDP} = \text{PDD} \times \frac{1}{f} = \frac{C_{\text{L}} \times \text{VDD}^2}{\text{f} \times \text{A}} \]

\[ \text{E-P satellite voltage drop, \theta = 0} \]
\[ \text{ADD-A} = 1.2 \text{V} \]
\[ \text{ADD-B} = 1.2 \text{V} \]

Super Buffer Design

\[ \text{chosen such that } C_{\text{MOS}} = C_{\text{N}} \text{ in the chain each inverter has an additional delay of} \]
\[ \frac{C_{\text{MOS}}}{C_{\text{N}}} \]

\[ \text{Thus} \quad \tau_{\text{total}} = \left( \frac{C_{\text{MOS}}}{C_{\text{N}}} \right) \tau_{\text{inverter}} \]
More generally, we can compute the energy it takes to charge a capacitance from a voltage $V_0$ to a voltage $V_2$. Using similar math, we derive that this requires an amount of energy equal to $C(V_2 - V_0)^2$. This equation will come in handy for a number of special circuits. One example is the NMOS pass-transistor chain. It is well-known that the minimum voltage at the end of such a chain is one threshold voltage below the supply [Roberts82]. Using the above-derived equation, we find that the energy dissipation in this case equals $C_{\text{pass}}(V_{\text{th}} - V_0)^2$, which is proportional to the swing at the output. In general, reducing the swing in a digital network results in a linear reduction in energy consumption.

**Slide 3.2**

Dynamic Power Consumption

Power = Energy per transition × Transition rate

$P = C V^2 f L_{\text{on}} = k V^2 L_{\text{on}}$

- $P$ = Power dissipation
- $V$ = Supply voltage
- $L_{\text{on}}$ = Switched capacitance
- $k$ = Activity factor

Power dissipation is data dependent and depends on the switching frequency, $f_{\text{on}}$, and the activity factor, $k$. The relationship between $P$ and $V^2$ is linear.

Consider a circuit with a clock frequency $f_c$. The probability that a node will be driven to a logic transition at a given clock tick is given by $p$, where $0 \leq p \leq 1$ is the activity factor at that node. As we discuss in the following slides, $p$ is a function of the circuit topology and the activity of the input signals. The accuracy of power estimation depends largely upon how well this activity is known—which is most often not the case.

**Slide 3.12**

This brings us back to the generic case of the CMOS inverter. To translate the derived energy per operation into power, it must be multiplied with the rate of power-consuming transitions, $f_{\text{on}}$. The unit of the resulting metric is Watt ($W$). The transition losses lead right away to one of the hardest problems in power analysis and optimization: it requires knowledge of the activities of the circuit. Consider a circuit with a clock frequency $f_c$. The probability that a node will be driven to a logic transition at a given clock tick is given by $p$, where $0 \leq p \leq 1$ is the activity factor at that node. As we discuss in the following slides, $p$ is a function of the circuit topology and the activity of the input signals. The accuracy of power estimation depends largely upon how well this activity is known—which is most often not the case.
Slide 3.13
Let us, for instance, derive the activity of a two-input NOR gate (which defines the topology of the circuit). Assume that such input has an equal probability of being a 1 or a 0 and that the probability of a transition is a clock tick is 30–99 as well, giving an even distribution between states. With the aid of the truth tables we derive that the probability of a 0-1 transition (or the activity of this 3-10) is 1.5. Moreover, the activity of the output node can be expressed as a function of the log-probability of the inputs D and E:

\[ A_{out} = p \cdot (D + E) \]

Slide 3.14
A similar analysis can be performed for an XOR gate. The observed activity is a bit higher (1.4).

Slide 3.15
These results can be generalized for all basic gates.

Slide 3.16
The topology of the logic network has a major impact on the activity. It is clearly illustrated by comparing the activity of NAND (NOR) and XOR gates as a function of fan-in. The output-transition probability of a NAND gate goes very quickly to zero. The probability of the output being a 1 is indeed becoming smaller with increasing fan-in. An example of such a network is a memory-address decoder. On the other hand, the activity of an XOR network is independent of fan-in. This does not relate well for the power dissipation of memories such as large complex memory elements, which primarily consist of NORs.

Slide 3.18
Another interesting logic family is the dynamic logic. The latter being smaller in dynamic logic. In general, though, the higher activity outweighs the capacitance gain.

Differential Logic?

Differential logic is a new logic family which may seem attractive for very low-power designs due to its increased signal-to-noise ratio. Differential implementations are, unfortunately, with an inherent disadvantage from a power perspective. Not only is the overall capacitance higher; the activity is higher as well (for both static and dynamic implementations). The only positive argument is that differential implementation reduces the number of gates needed for a given function, and thus reduces the length of the critical path.
static power analysis seem favorable at a first glance. Consider, for instance, the network shown on the slide, and assume that for 1 and 0 probabilities of the primary input signals are known. Using the basic circuit analysis procedures outlined in the previous section, the output signal probabilities can be computed for the first layer of gates coming from the primary inputs. This process is then repeated with the primary outputs as inputs to the next layer. These reasoning steps lead to a straightforward result. However, there is a catch: for the basic gate equations to be valid, the inputs cannot be statistically independent. In probability theory, we say that two events are statistically independent if the occurrence of one event makes it equally likely that the other occurs. While this assumption is in general true for the network of the slide assuming obviously that the primary input signals are independent, it is unfortunately rarely holds in actual circuits.

Temporal Correlations

- Feedback and temporal correlations
- *Out of phase correlations
- Feedback and temporal correlations
- *Out of phase correlations

**Slide 3.20**

State the primary inputs to a logic network are independent, the signals may become correlated or dependent, while the power dissipation through the logic network. This is best illustrated with a simple example, which shows the impact of a network property called temporal correlation. The network has a NAND gate 2 in the rightmost circuit, and the NAND gate 2 is not independent, but are both functions of the same input signal 2. To compute the output probability of 2, the expressions derived earlier apply. For a NAND gate, it is also the probability of some event, i.e., given the occurrence of some other event. Conditional probability is the probability of some event given another event, and in this example, the probability of 2, given 1. More specifically, one can derive that \( p(2|1) = \frac{p(2,1)}{p(1)} \), assuming that \( p(2,1) \neq 0 \). When propagating these conditional probabilities through the network non-terminally possible, you may find that the complexity of doing so for complex networks rapidly becomes unmanageable, and that indeed is the case.

**Slide 3.21**

The story gets complicated even further by the occurrence of temporal correlations. A signal shows temporal correlation if a data value in the signal stream is dependent upon previous values in the stream. Temporal correlations are the norm in sequential networks, as any signal in the network is typically a function of its previous values, and is affected by the existence of feedback network. In addition, primary input signals as well may show temporal dependence. For example, in a digitized speech signal any sample value is dependent upon the previous values.

All these arguments help illustrate that static activity analysis is a very hard problem indeed, and actually, all but impossible. Hence, power analysis tools either rely on simulations of actual signal traces to derive the signal probabilities or make simplifying assumptions—for instance, it is assumed that the input signals are independent and jointly random. This is discussed in more detail in Chapter 12. In the following chapters, we will most often assume that activity of a module in its typical operation mode can be characterized by an independent parameter.
\[ N = 4 \quad \varphi = \alpha_1 (\omega_0 + \omega_1) \varphi_0 \left( 1 + \omega_1 + \omega_1^2 + \omega_1^3 \right) \]

**Active area:**
\[
= \frac{\sum_{k=0}^{N \varphi} (\omega_0 + \omega_1) \omega_1^k}{\sum_{k=0}^{N \varphi} (\omega_0 + \omega_1) \omega_1^k}
\]

\[ N = 4 \quad \varphi = \alpha_2 (\omega_0 + \omega_1) \varphi_0 \left( 1 + \omega_1^2 + \omega_1^3 + \omega_1^4 \right) \]

**Active area:**
\[
= \frac{\sum_{k=0}^{N \varphi} (\omega_0 + \omega_1) \omega_1^k}{\sum_{k=0}^{N \varphi} (\omega_0 + \omega_1) \omega_1^k}
\]