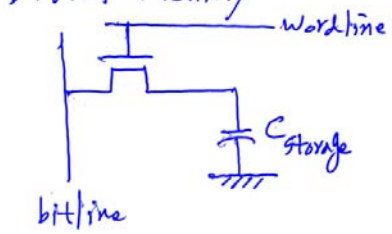
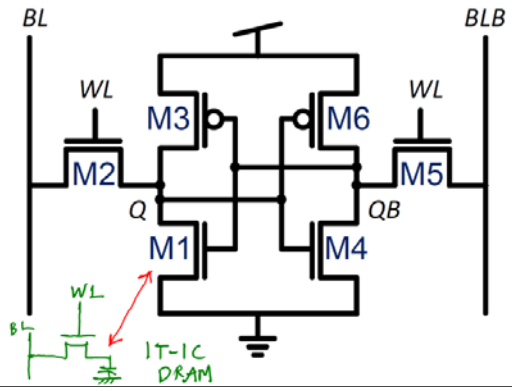
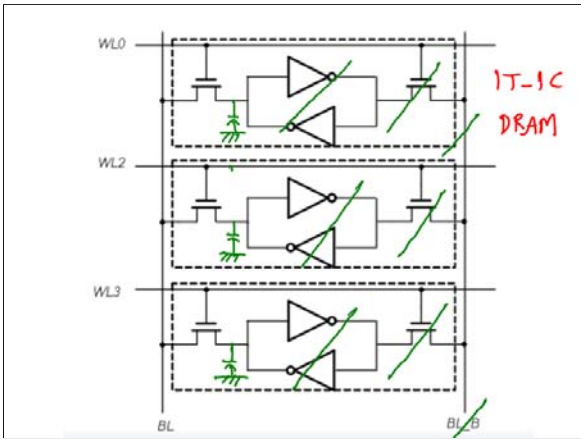
EE 222 Lecture 7 Jan 30, 2017

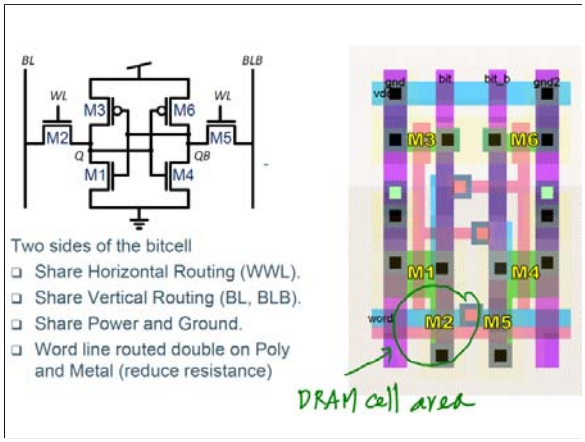
DRAM Memory

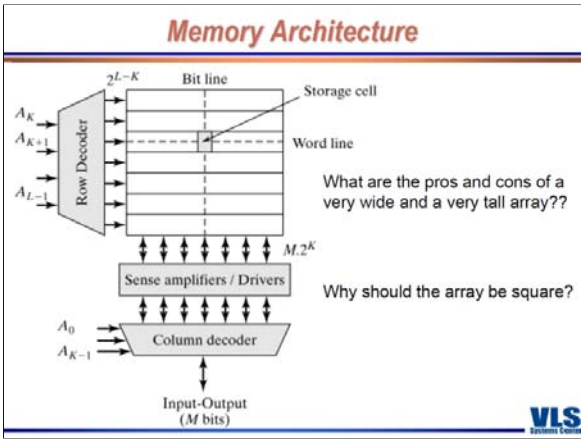


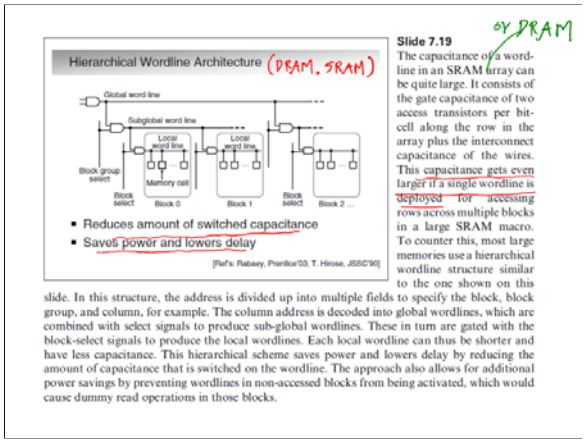
6-transistor SRAM cell





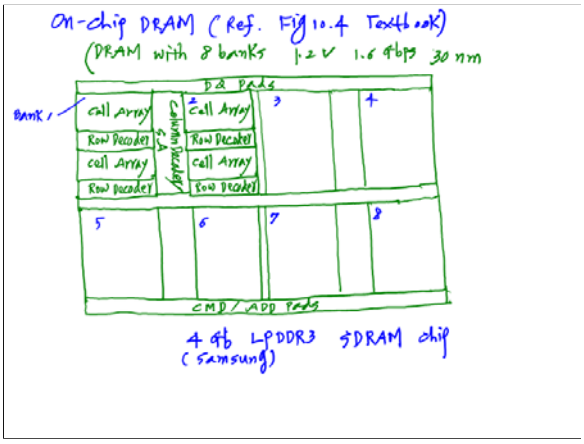


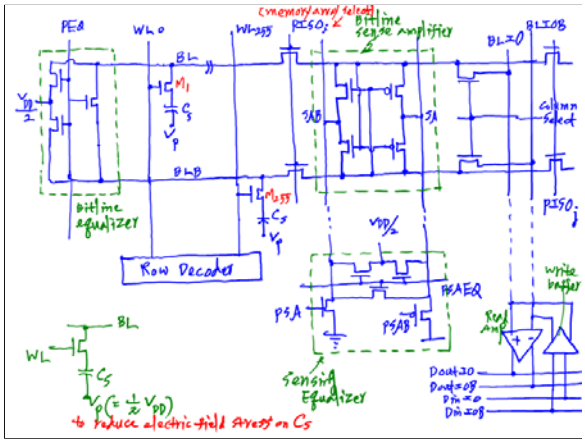




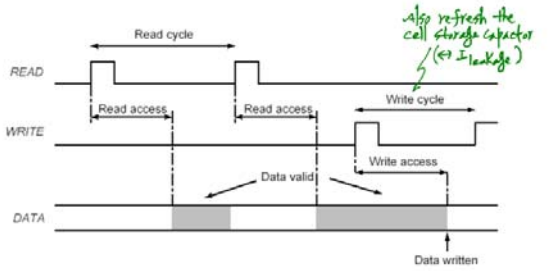
Slide 7.19

The capacitance of a word-line in an SRAM array can be quite large. It consists of the gate capacitance of two access transistors per bit-cell along the row in the array plus the interconnect capacitance of the wires. This capacitance gets even larger if a single wordline is deployed for accessing rows across multiple blocks in a large SRAM macro. To counter this, most large memories use a hierarchical wordline structure similar to the one shown on this slide. In this structure, the address is divided up into multiple fields to specify the block, block group, and column, for example. The column address is decoded into global wordlines, which are combined with select signals to produce sub-global wordlines. These in turn are gated with the block-select signals to produce the local wordlines. Each local wordline can thus be shorter and have less capacitance. This hierarchical scheme saves power and lowers delay by reducing the amount of capacitance that is switched on the wordline. The approach also allows for additional power savings by preventing wordlines in non-accessed blocks from being activated, which would cause dummy read operations in those blocks.



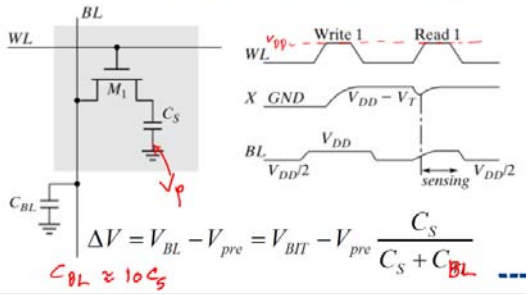


Memory Timing: Definitions



1-Transistor DRAM Cell

- Data is dynamically stored on C_S.
- Read is destructive. Write back is necessary



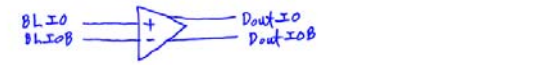
$$\Delta V = V_{BL} - V_{pre} = V_{BIT} - V_{pre}\frac{C_S}{C_S + C_{BL}}$$

$C_{BL} \approx 10 C_S$

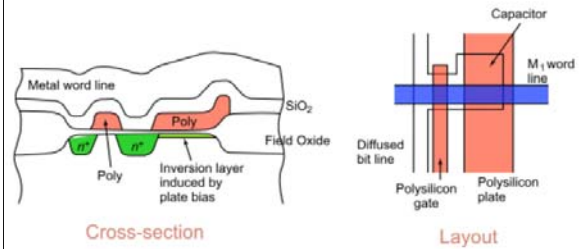
Recall Power consumption

- $P = \alpha C V_{DD} \Delta V f_{clock}$, $\alpha \leq 1$

  $P \propto \Delta V$; the smaller ΔV, the less P
- For signal integrity, differential sense amplifier (SA) is used to read '0' or '1'



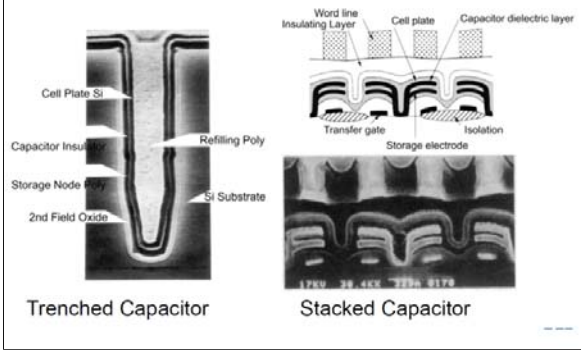
1-Transistor DRAM Cell



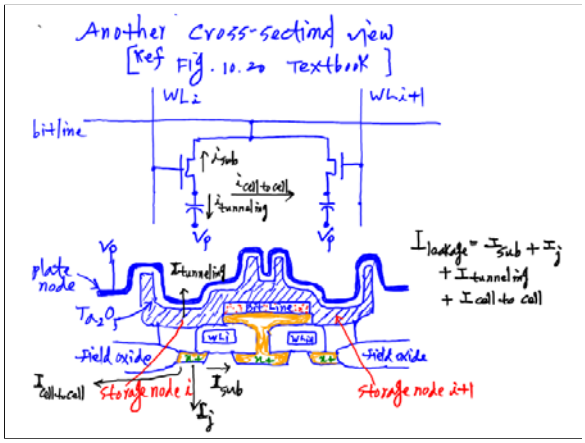
Uses Polysilicon-Diffusion Capacitance

(−) Expensive in Area

Advanced 1T DRAM Cells

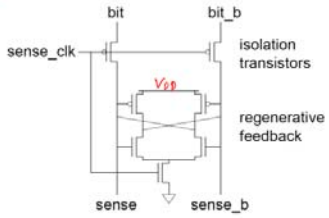


Trenched Capacitor Stacked Capacitor

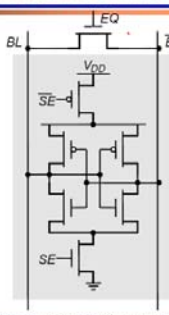


Clocked Sense Amplifier

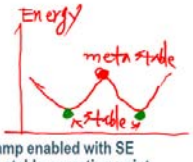
- Clocked sense amp saves power
- Requires sense_clk after enough bitline swing
- Isolation transistors cut off large bitline capacitance



Latch-Based Sense Amplifier (DRAM)

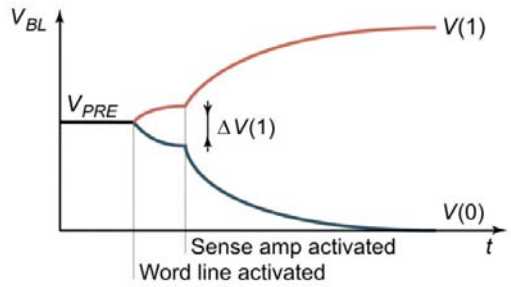


One side connected to a dummy Bitline with a discharged cell connected as a reference and to increase swing



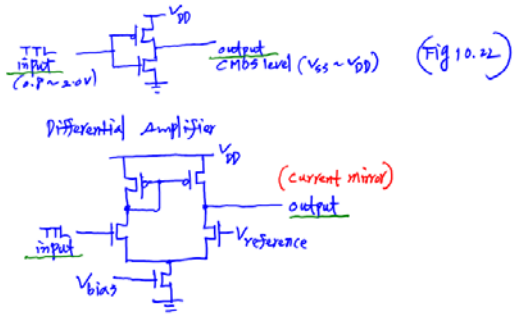
Initialized in its meta-stable point with EQ
Once adequate voltage gap created, sense amp enabled with SE
Positive feedback quickly forces output to a stable operating point.

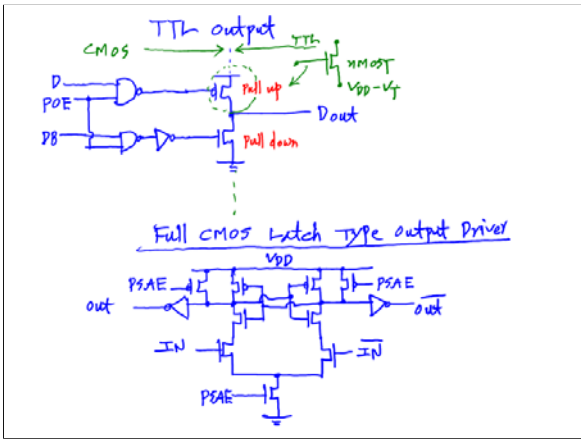
Sense Amp Operation

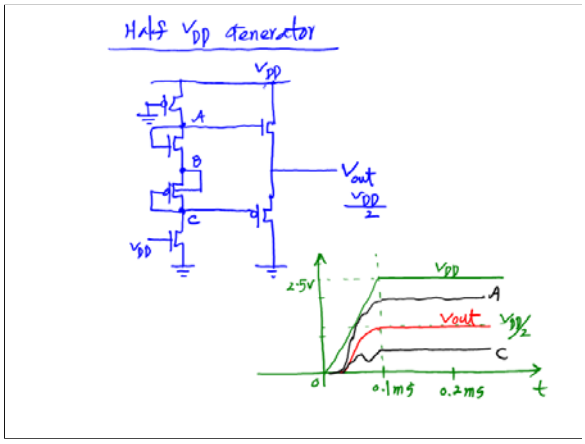


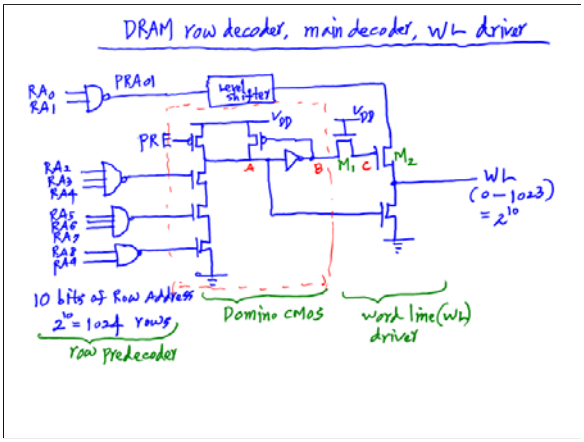
DRAM I/O circuits (Textbook sect 10.2)

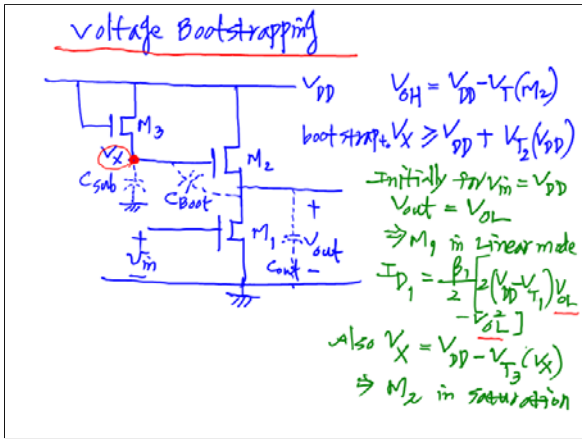
TTL (bipolar) signals 0.8 ~ 2.0 V
CMOS at a different level











$I_{D_2}=\frac{\beta_2}{2}\left[V_X-V_{OL}-V_{T_2}\right]^2$

$I_{D_1}=I_{D_2} \Rightarrow V_{OL}$ solve for

$C_{boot} \simeq C_{gs}(M_2)$

Boot strapping when $V_{in}: V_{DD} \to 0$

$\Rightarrow V_{out}: V_{OL} \nearrow$ (charged through M_2)

$\frac{dV_{out}}{dt}>0$ is coupled to node X to increas $V_X \Rightarrow V_{out} \nearrow V_{DD}$

$\frac{dV_X}{dt}=\frac{C_{boot}}{C_{boot}+C_{sub}}\frac{dV_{out}}{dt}$

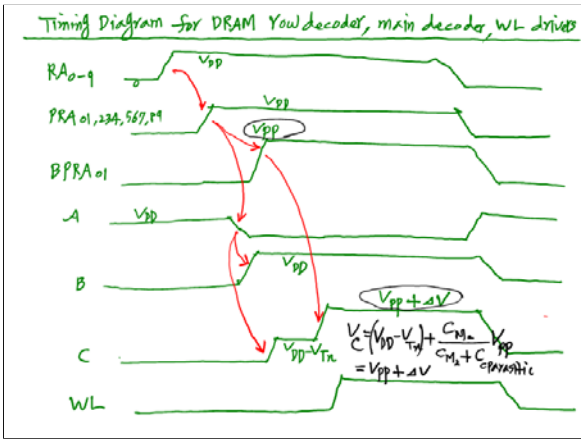
$$\int_{V_{DD}-V_{T_3}}^{V_X^{max}} dV_X = \frac{C_{boot}}{C_{boot}+C_{sub}} \int_{V_{OL}}^{V_{DD}} dV_{out}$$

$$V_X^{max} = V_{DD}-V_{OL}+V_{DD}-V_{T_3}$$
$$= V_{DD}-V_{T_3}+\gamma(V_{DD}-V_{OL})$$

where $\gamma = \frac{C_{boot}}{C_{boot}+C_{sub}}$

If $C_{boot} \gg C_{sub}$, then $\gamma=1$

$V_X^{max} = 2V_{DD}-V_{T_3}$



Midterm Exam on Feb. 6

1) open book, open computer test
2) study HW problems, lecture notes calculation of numerical values for C, V_T, I, etc.
3) Derivation of circuit optimization

Proposal due on Feb 6 (in writing)