EE222 Lecture 8  Feb 1, 2018

ROM (Read Only Memory) - NOR ROM

\[
\begin{align*}
\bar{x}_1 &= \bar{x}_2 + \bar{x}_3 \\
\bar{x}_2 &= \bar{x}_4 + \bar{x}_5 \\
\bar{x}_3 &= \bar{x}_4 + \bar{x}_5 \\
\bar{x}_4 &= \bar{x}_3 + \bar{x}_5 \\
\bar{x}_5 &= \bar{x}_3 + \bar{x}_4 \\
\end{align*}
\]

NOR decoder - NOR ROM ARRAY

4x4 NOR-based ROM

An Example of Column Decoder Circuit (Binary Tree Decoder)
A Structure of CMOS Dynamic PWA (Layout)

\[ C_{\text{H}} = \frac{b (C_{\text{drive}} + N \cdot C_{\text{min}})}{V_{\text{SS}}} \leq C_{\text{spec}} \]

For \( C_{\text{spec}} = 2.5 \times 10^{-13} \) (nano-Farads)

- \( C_{\text{drive}} = 0.1 \times 10^{-12} \)
- \( N = 1 \times 10^{-12} \)
- \( b = 2 \) (empirical constant)
- \( V_{\text{SS}} = 0.6 \times 10^{-12} \)
- \( C_{\text{min}} = 1 \times 10^{-12} \)

\[ N < \frac{0.25 \times 10^{-12} \times 6.6 \times 6.6 	imes 0.15 \times 10^{-12}}{2 \times (0.6 \times 10^{-12}) \times 10^{-12} \times 2.4 \times 10^{-12} \times 10^{-12}} \]

\( \approx 62 \) (number of nMOS per pMOS)

Nonvolatile Semiconductor Memory

Metal-Insulator-Semiconductor (MIS) Structure
**Operation Principle of Nonvolatile Memory**

Metal - Insulator - Metal Insulator - Semiconductor

Electrons are injected into the 'floating gate' by tunneling through the insulator, and are stored semi-permanently.

**MNOS Structure (Metal Nitride Oxide System)**

- Metal
- Nitride
- Oxide
- Substrate

Electrons are injected into the nitride layer by applying a voltage, and are released by applying a voltage to the metal gate. (Vg)

**Energy Band Diagram**

- M (Metal)
- N (Nitride)
- Oxide
- S (Semiconductor)

- Forward bias
- Reverse bias

**Stacked Oxide Tetradile Proposed by H. S. Bill & T. W. Tanks (1989)**

- Effect gate (91)
- Central gate (9f)
- Deflection & Scan Substrate

**Equations**

\[ J_n = \frac{C_n E_n^2}{2\kappa} \exp \left( - \frac{E_n}{E_{ox}} \right) \]

\[ J_{ox} = \frac{C_{ox} E_{ox}}{\sinh \left( \frac{k T}{E_{ox}} \right)} \exp \left( - \frac{E_{ox}}{E_{ox}} \right) \]

- \( E_n \) = electric field in the nitride layer
- \( E_{ox} \) = oxide layer
- \( z \) = Boltzmann constant
- \( T \) = temp in [°K]

**Note**: Use SI units for all calculations.
Flash Memory

Memory cell is a transistor with a floating gate whose threshold voltage can be programmed (changed) repeatedly by applying an electric field (through $V_g$ voltage) to the gate.

$\Delta V_t (c_e) = \frac{-\Delta q}{C_{pe}}$

$V_{ctrl}$

Control gate voltage $V_C$

$V_{data} = V_{data} + \frac{V_{ctrl}}{C_{pe}}$

$V_{data} = V_{data} + \frac{\Delta q}{C_{pe}}$

Charge pumping for high voltage $V_{pp}$ generation

Multi-level cell threshold voltage distribution in Flash (for values - 2-bit/cell)
Slide 11.4
Although knowing the power density constant is one motivation for the continued search to lower the IOP, another, maybe even more important, reason is the exciting applications that only become feasible at very low power levels. Consider, for instance, the digital wrist watch. The concept, though straightforward, only became attractive once the power dissipation

\[ \text{Subthreshold Operation} \]

Opportunities for Ultra-Low Voltage

- Number of applications emerging that do not need high performance, only extremely low power dissipation
- Examples:
  - Steady-state operation for mobile components
  - Implanted electronics and artificial senses
  - Small objects, home, and e-textiles
- Need power levels below 1 mW (even μW in certain cases)

\[ V_{DD} = I_0 \times e^{(V_{DS} - V_{th})} \left( 1 - \frac{1}{e^{(V_{DS} - V_{th})}} \right) \]

where

\[ I_0 = \frac{V_{DS} - V_{th}}{e^{(V_{DS} - V_{th})} \left( 1 - \frac{1}{e^{(V_{DS} - V_{th})}} \right)} \]

Slide 11.6

For monolithic design, there are several techniques that can lead to lower power consumption. One such technique is the use of subthreshold operation. The subthreshold current, given by

\[ I_{sub} = \frac{V_{DD} \times \mu C_{ox} \times W}{L} \times \left( 1 - \frac{1}{e} \right) \]

where

\[ \mu = \frac{\text{mobility}}{\text{temperature}} \]

thermal voltage leads to transistors having higher margins (assuming \( \mu = 1 \)). This is approximately equal to \( V_{th} \).

Slide 11.7

Calculating the voltage transfer function (VTF) of an inverter is derived by operating the current through the subthreshold region.

\[ A_{VTF} = \frac{V_{DD} \times \left( 1 - \frac{1}{e} \right)}{V_{th}} \]

\[ V_{th} = \frac{1}{\mu C_{ox} \times W/L} \]

\[ V_{DD} = x \times V_{th} \]

\[ x = \frac{1}{1 - \left( \frac{1}{e} \right)} \]

\[ k = \frac{1}{V_{th}} \]

\[ A = \frac{1}{k} \times \left( 1 - \frac{1}{e} \right) \]

\[ X_0 = \frac{V_{th}}{V_{DD}} \]

Results from Analytical Model

Sub-threshold Inversion

Normalized VTH vs. transfer function of an inverter

Current-voltage curves for a given value of threshold voltage before and after optimization

\[ V_{th} = 0.1 \text{ threshold voltage} \]

\[ x = 1 \text{ for } V_{th} = 0.1 \text{ threshold voltage} \]

\[ V_{th} = \frac{1}{2} \text{ thermal voltage} \]

\[ V_{th} = 0.25 \text{ thermal voltage} \]

\[ V_{th} = 0.5 \text{ thermal voltage} \]

\[ V_{th} = 0.75 \text{ thermal voltage} \]

Continued-by-Simulation (at 60 nm)

Minimum operational voltage

Maximal operational voltage

Observe, as the VTH increases, the minimum operational voltage decreases. This is typically referred to as the "critical" or "operational" point. As such, the inverter is only marginally functional. In the simulations, we assume a yield of approximately 75%.
GRAND CHALLENGES IN THE NEAR-TERM (THROUGH 2020) AND LONG-TERM (2021 AND BEYOND)

LOGIC DEVICE SCALING (PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FINE-GRANULARITY PROCESSES, MODELING AND SIMULATION, AND METHODOLOGY)

The continued use of existing CMOS technology, however, faces significant challenges such as power and performance requirements.

The introduction of high-mobility transistors (HBT) is expected to be a significant improvement in the near-term despite the introduction of high-performance transistors (HPT). Integration of high-performance transistors will further improve the performance of digital circuits, thereby reducing the power consumption.

High-quality silicon materials, however, have been considered as an enhancement or replacement for Si transistors for CMOS logic applications. High-performance transistors with low on-state resistance (ON), low-off leakage, and high field-effect mobility are expected. A particularly promising approach is the use of the HEMT (High Electron Mobility Transistor) and SOI (Silicon On Insulator) devices.

MEMORY DEVICE SCALING (PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FINE-GRANULARITY PROCESSES, MODELING AND SIMULATION, AND METHODOLOGY)

The challenges for DRAM devices in logic applications, such as the 24000MB DRAM, have been recognized as a key aspect in the near-term. Continued improvements in the near-term need to be addressed in this regard.

High-quality substrates have been considered as an enhancement or replacement for Si transistors for CMOS logic applications. High-performance transistors with low on-state resistance (ON), low-off leakage, and high field-effect mobility are expected. A particularly promising approach is the use of the HEMT (High Electron Mobility Transistor) and SOI (Silicon On Insulator) devices.