EE222 Midterm Examination solution

February 6, 2018

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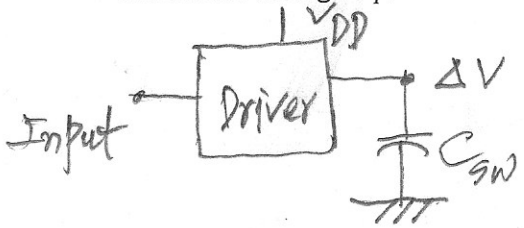
1. (20 points) For low power operation of CMOS circuits, **describe the design principle** in terms of power supply voltage V_{DD}, voltage swing ΔV at output nodes, switched capacitance C_{sw}(= product of switching frequency and capacitance), and MOST's threshold voltage V_T.



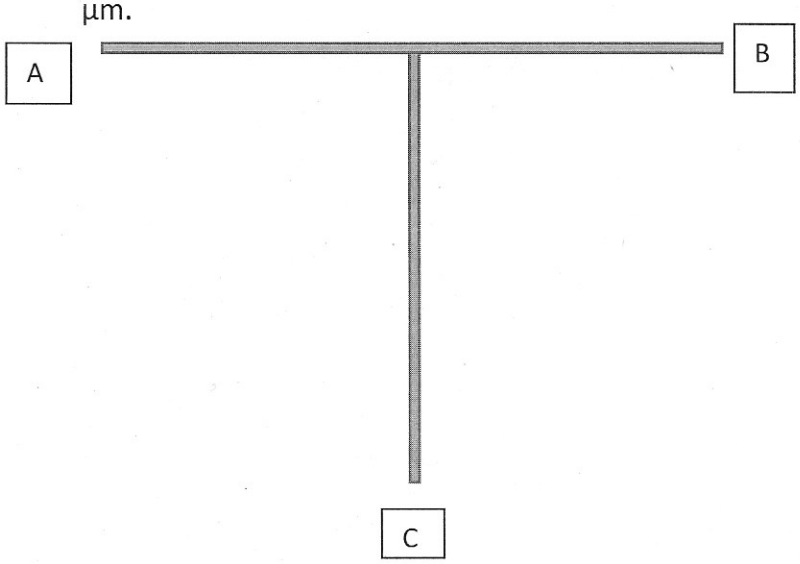
i) Power = switching (dynamic) power + short-circuit power + leakage power.

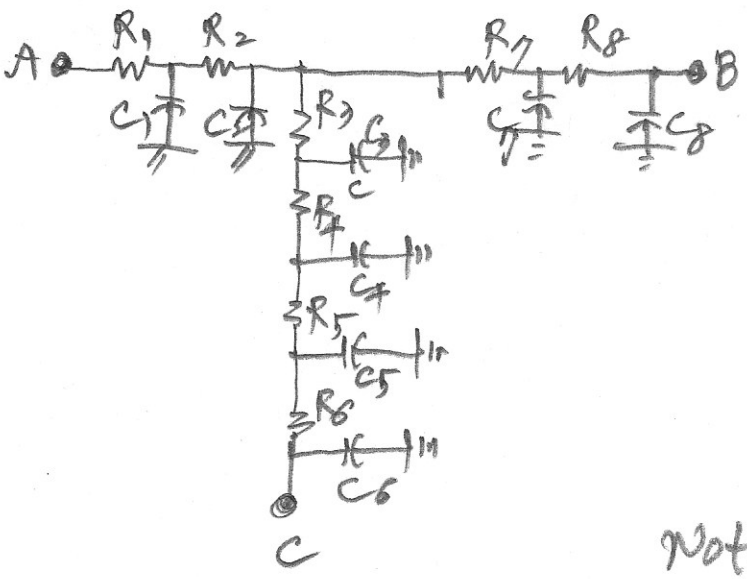
ii) $P_{sw} = \alpha C_{sw} V_{DD} \Delta V f_{clock}$
- Thus lowering V_{DD}, as long as delay specification are met, is of critical importance
- Lowing ΔV so long as logic states can remain correct is also important
- C_{sw} should be lowered through careful layout and minimization of interconnect parasitics
- αf_{clock} should be also lowered, which often takes logic changes.

iii) For leakage power minimization, V_T should not be lowered too much, and lowering V_{DD} is also important.

iv) For minimization of short circuit power, the slew rates of input signals, output signals should be lowered so that the duration in which both PMOSTs and NMOSTs are simultaneously should be minimized.

2. (20 points) Let us consider a T shape metal interconnect configuration of a uniform width 1 μm that connects three gates. Its horizontal length from point A to point B is 1000 μm and its vertical length starting at the center of the horizontal line is also 1000 μm long ending at point C.
Assuming that the line resistance is 0.1 Ω/square, and line capacitance including the fringing field effect is 0.066 fF/ μm^2, **find an Elmore delay from the top left corner point A to the bottom most point C.** Use a distributed L-type RC model for every 250 μm.





Elmore delay τ_{ac}

$= R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3$
$+ (R_1+R_2+R_3+R_4)C_4$
$+ (R_1+R_2+R_3+R_4+R_5)C_5$
$+ (R_1+R_2+R_3+R_4+R_5+R_6)C_6$
$+ (R_1+R_2)C_7 + (R_1+R_2)C_8$

Note that $R_K = R_0, \forall K$

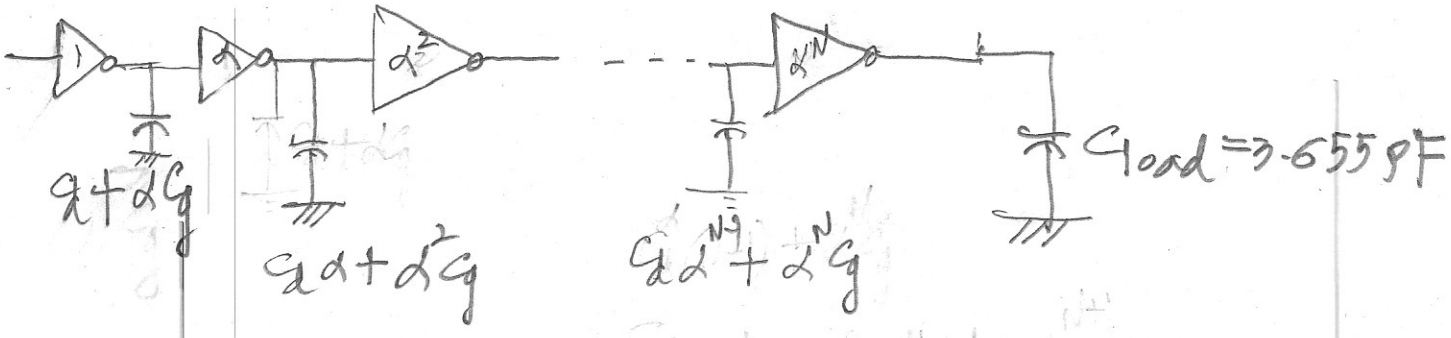
$C_K = C_0, \forall K$

$R_0 = 250\ \square_\Omega \times 0.1\ \Omega/\square = 25\ \Omega$

$C_0 = 250\ \mu m^2 \times 0.066\ fF/\mu m^2$
$= 16.5\ fF$

thus, $\tau_{ac} = R_0C_0[1+2+3+4+5+6+2+2]$
$= 25 \times 16.5 \times 10^{-15} \times 25 = \underline{10.31\ ps}$ ans

3. (30 points) A super buffer can be used to drive a large load capacitance C_{load} instead of abruptly enlarging the driving gate's transistor sizes. When the gate capacitance of an intrinsic inverter is C_g =0.166 fF and C_{load}= 3.655 pF,
find a minimum delay in picoseconds. Here the intrinsic inverter's delay τ_o is calculated from a 11-stage ring oscillator that has a frequency of 90.9 GHz.
(Hint: Find τ_o from the oscillation frequency as f= 1/(2 X 11τ_o). Also $C_{load}/C_g = e^{10}$ with e= 2.718.)



$C_{load} = C_d \alpha^N + \alpha^{N+1} C_g$

$C_d \ll C_g$, thus $C_{load} \cong \alpha^{N+1} C_g$ $\quad \therefore \alpha^{N+1} = \frac{C_{load}}{C_g}$

For minimum delay $\alpha = e$ and thus $(N+1) = \ln \frac{C_{load}}{C_g}$

$= \ln e^{10} = 10$ $\quad \boxed{N+1 = 10}$

Total delay $= (N+1)\,\tau_o\, e$

$\cong 10\,\tau_o\, e$

where τ_o is the delay of an inverter in the 11-stage ring oscillator $\Rightarrow$ $\tau_o = \frac{1}{2 \times 11 \times 90.9 \times 10^9} = 0.5$ ps

$\tau_{Superbuffer} = 10\,(0.5\text{ ps})\,2.718 \cong 13.59$ ps

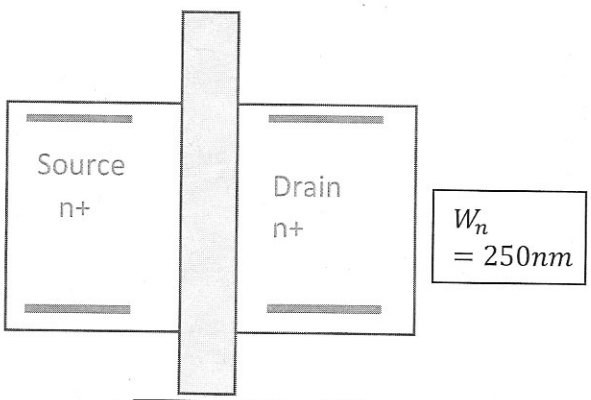
ans

4. ~~after wordline (gate voltage) is switched to $2V_{DD}$~~. (30 points) A dynamic random access memory (DRAM) cell is connected to its bitline (BL) with a total capacitance of 450 fF. The physical dimensions of the DRAM cell's NMOS transistor is shown below. The current driving power I_{DS} is described below. Let us assume that $V_{DD} = 2V$ and V_{Tn}= 0.5 V, $C_{storage}$= 50 fF. **Find the time it takes for BL, which was precharged to $\frac{V_{DD}}{2}$ by a precharge pulse while $C_{storage}$ was charged to V_{DD}, to reach the beginning of a steady state value after the wordline (WL) signal which is the gate voltage of NMOS transistor is switched to $2V_{DD}$.**

For simple calculation, assume that the parasitic drain capacitance can be neglected, and WL is driven with a high voltage 2 V_{DD} such that the NMOST is in its linear region, i.e.,

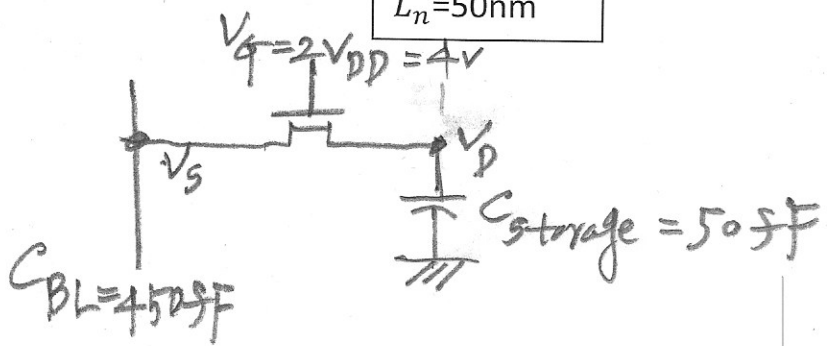
$$I_{DS} = k_n' W_n/L_n \frac{1}{1+\frac{V_{DS}}{E_C L_n}} ((V_{GS} - V_{Tn}) V_{DS} - \tfrac{1}{2} V_{DS}^2),$$

where $E_C = 10^5$V/cm, L_n = 0.05 μm. The average value of $I_{DS} = \frac{1}{2}$(I_{DS} for V_{DS}= 2V + I_{DS} for V_{DS}= steady state value) can be used for calculation of the delay.



Source is connected to BL with its capacitance of 450 fF

Drain is connected to the storage capacitance of 50 fF



Initially V_S $\frac{1}{2}V_{DD} = 1$ V_D $V_{DD} = 2V$ V_{DS} 1 V

Finally 1.1 V 1.1 V 0 V

after charge redistribution

$V_{final} = \frac{450fF \cdot 1 + 50fF \cdot 2}{450fF + 50fF}$

$= 0.9 + 0.2 = 1.1V$

$I_{DS_{avg}} = \frac{1}{2} I_{DS}\Big|_{V_{DS}=1V}$

$V_{GS} = 4 - (1 \sim 1.1) = 3.9 \sim 4.0$

But when $V_{GS} = 3.9$, $V_{DS} = 0$

thus we can assume $V_{GS} = 4$

(for problem 4 continuation)

Thus $I_{DS} = K_n' \frac{W_n}{L_n} \frac{1}{1 + \frac{V_{DS}}{E_C L_n}} \left((V_{GS} - V_{Tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$

$= K_n' \left(\frac{250\,nm}{50\,nm} \right) \frac{1}{1 + \frac{1\,V}{10^5 \frac{V}{cm} \times 0.05 \times 10^{-4}\,cm}}$

$\times \left((3 - 0.5) 1 - \frac{1}{2} 1^2 \right)$ for $V_{DS} = 1$

$I_{DS\,avg} = \frac{1}{2} \left\{ K_n' (5) \frac{1}{1 + \frac{1}{0.5}} (2.5 - 0.5) \right\}$

$= K_n' \frac{5 \times 1}{1 + 2} = K_n' \frac{5}{3}$

$\tau = \frac{\Delta Q}{I_{DS\,avg}} = \frac{450\,fF \times 0.1\,V}{K_n' \frac{5}{3}} = \frac{45\,f\,Coulomb}{K_n'} \times 0.6$

$= \boxed{\frac{27\,fC}{K_n'}}$

If we use $K_n' = 280\,\mu A/V^2$ for 45 nm tech,

$\tau = \frac{27 \times 10^{-15}\,C}{280 \times 10^{-6}\,A} = 0.096\,ns$ ans