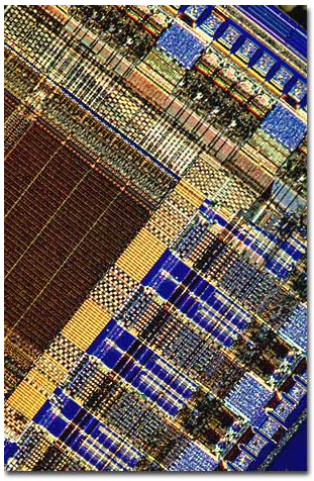
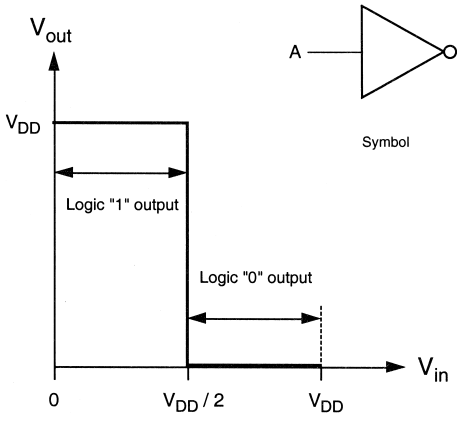
CMOS Digital Integrated Circuits



Chapter 5
MOS Inverters: Static Characteristics

Y. Leblebici

Ideal Inverter



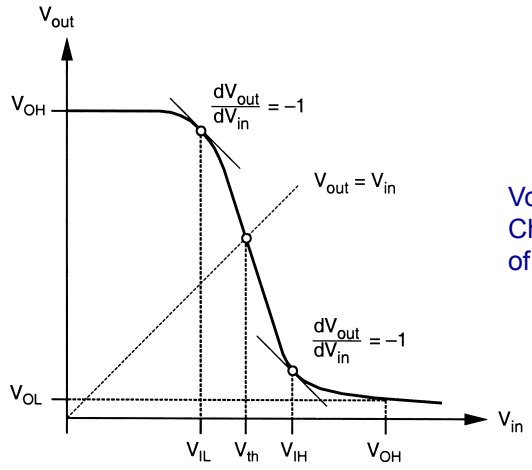
Symbol

A	B
0	1
1	0

Truth Table

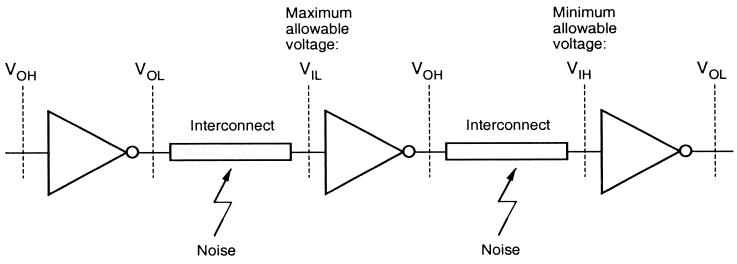
Voltage Transfer Characteristic (VTC) of the ideal inverter

Generic Inverter VTC



Voltage Transfer Characteristic (VTC) of a typical inverter

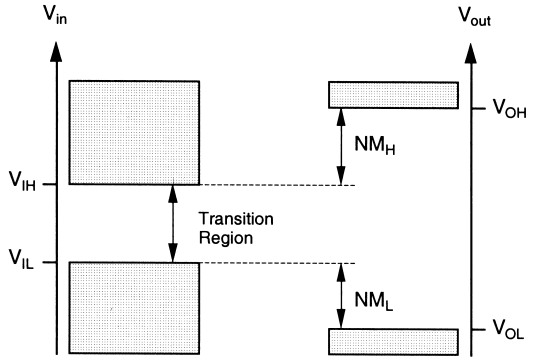
Noise Margins



Propagation of digital signals under the influence of noise

- V_{OH} : $V_{OUT,MAX}$ when the output level is logic "1“
- V_{OL} : $V_{OUT,MIN}$ when the output level is logic "0“
- V_{IL} : $V_{IN,MAX}$ which can be *interpreted* as logic "0“
- V_{IH} : $V_{IN,MIN}$ which can be *interpreted* as logic "1"

Noise Margins



Definition of
noise margins

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$

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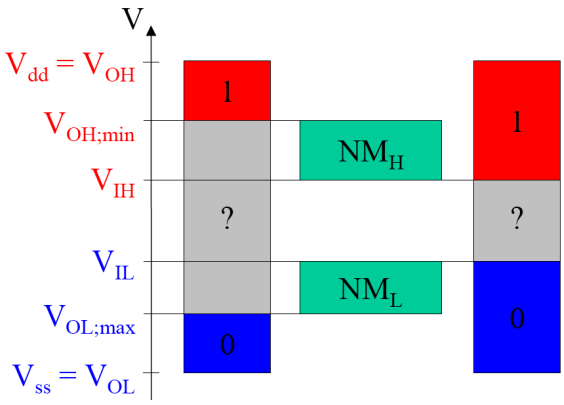
Noise Margins



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Noise Margins

Nominal output $V_{out} = f(V_{in})$

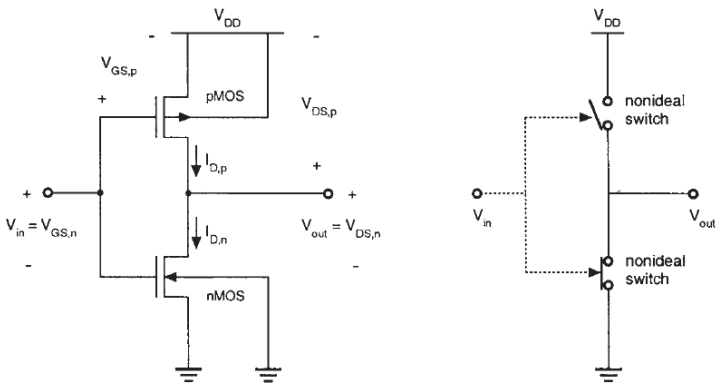
Output under noise $V'_{out} = f(V_{in} + \Delta V_{noise})$

$$V'_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise} + \text{higher order terms (neglected)}$$

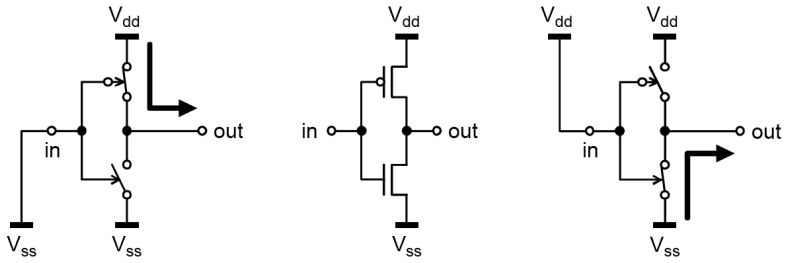
$$\text{Perturbed Output} = \text{Nominal Output} + \text{Gain} \times \text{External Perturbation}$$

The nominal operating region is defined as the region where the gain is less than unity !

CMOS Inverter Circuit



CMOS Inverter Circuit



The NMOS switch transmits the logic 0 level to the output, while the PMOS switch transmits the logic 1 level to the output, depending on the input signal polarity.

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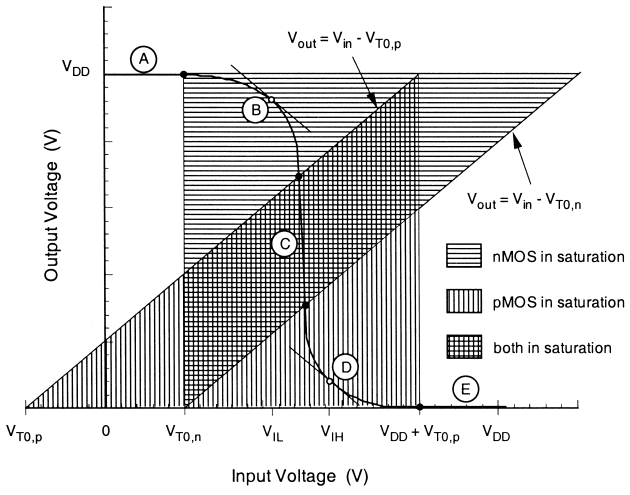
CMOS Inverter Circuit



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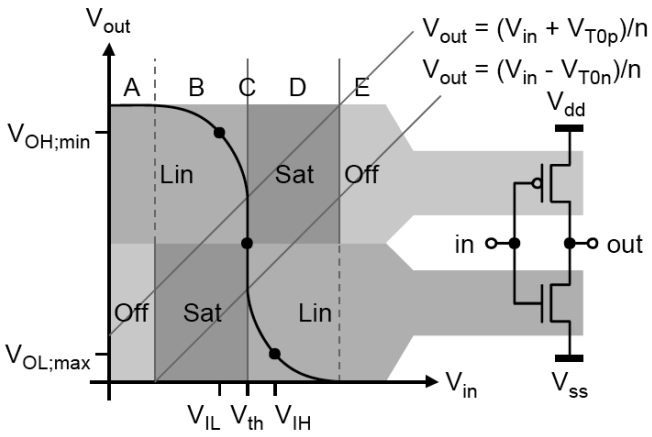
CMOS Inverter Circuit



CMOS Inverter Circuit

determine noise margins

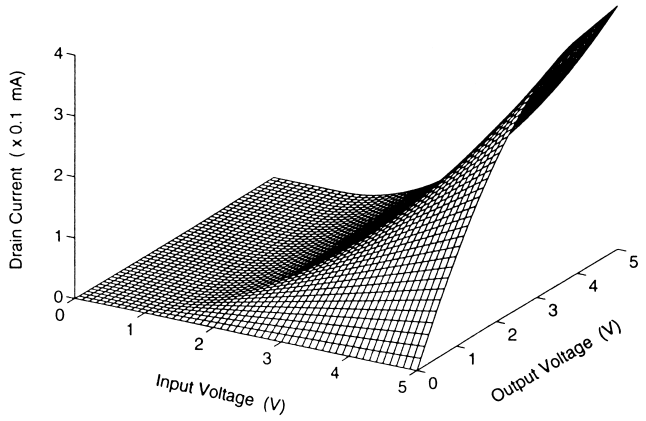
$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \qquad (5.62)$$

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot (2V_{out} + V_{T0,n})}{1 + k_R} \qquad (5.67)$$

inversion (switching) threshold voltage

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} + V_{T0,p})}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} \qquad (5.71)$$

CMOS Inverter Circuit



nMOS transistor current-voltage characteristics

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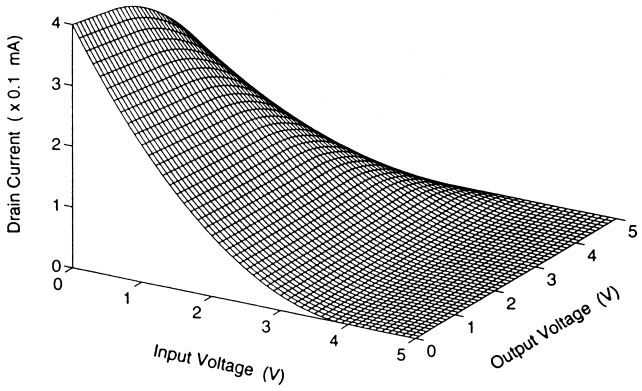
CMOS Inverter Circuit



pMOS transistor current-voltage characteristics

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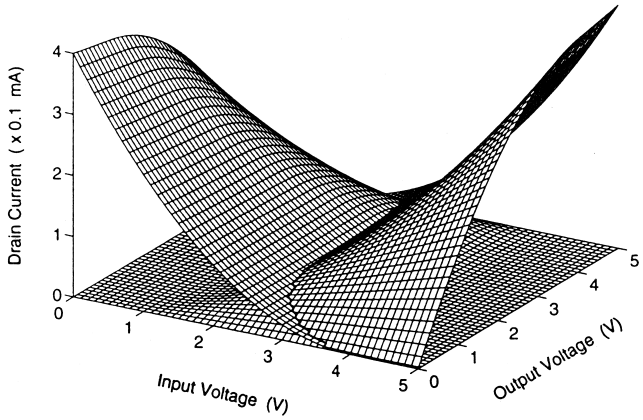
CMOS Inverter Circuit



Intersection of current-voltage surfaces of nMOS and pMOS transistors

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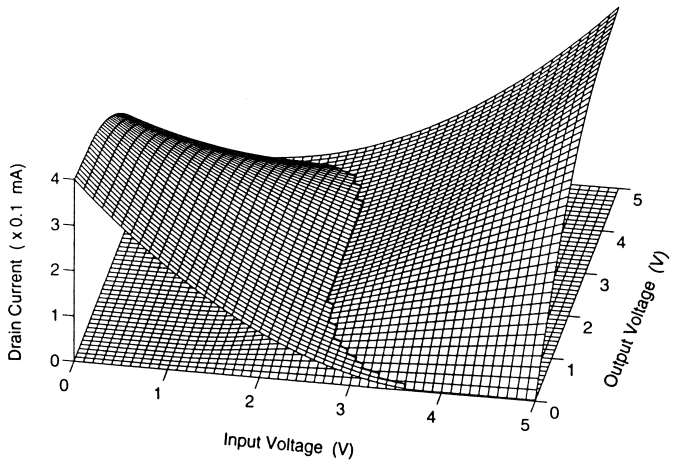
CMOS Inverter Circuit



Intersection of current-voltage surfaces gives the VTC in the voltage plane

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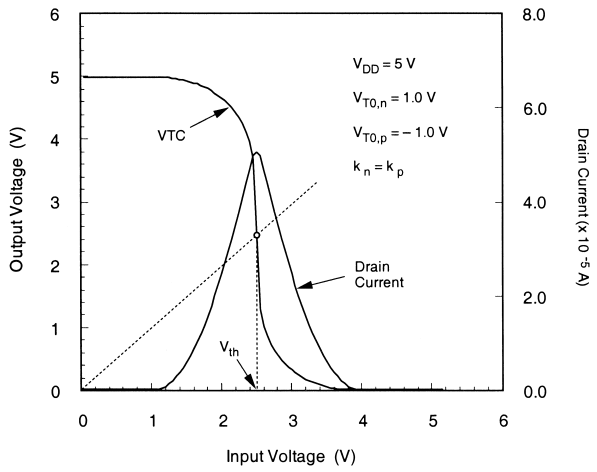
CMOS Inverter Circuit



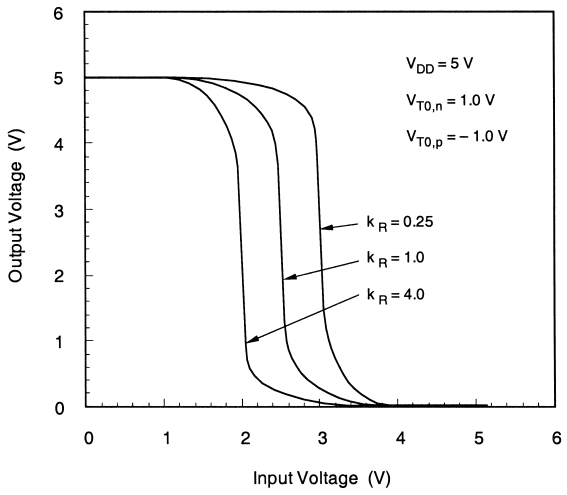
CMOS Inverter Circuit

How to choose the k_R ratio to achieve a desired inversion threshold voltage:

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2 \qquad (5.73)$$

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L} \right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L} \right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L} \right)_n}{\mu_p \cdot \left(\frac{W}{L} \right)_p} \qquad (5.77)$$

CMOS Inverter Circuit



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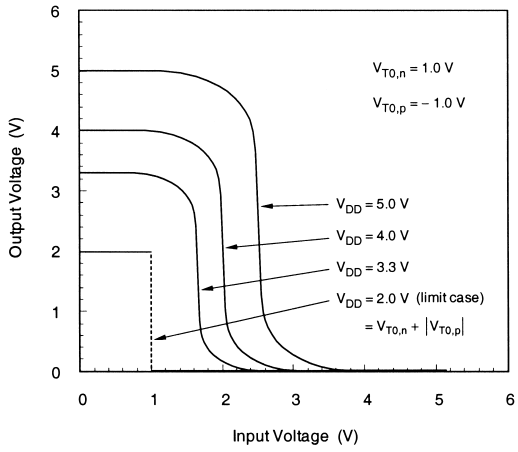
Supply Voltage Scaling



VTC of a CMOS inverter for different power supply voltage values.

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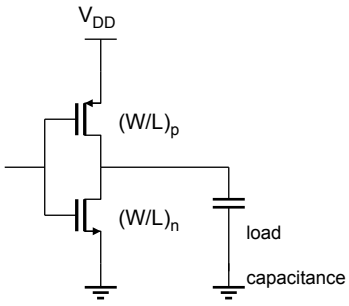
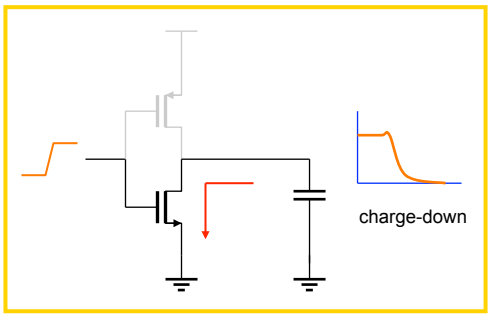
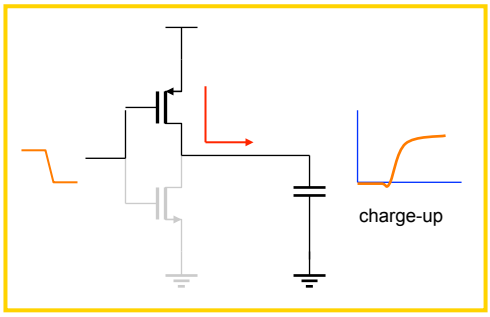
Dynamic Characteristics of CMOS Inverter







Switching speed determined by the time required to charge-up or charge-down the output load capacitance.

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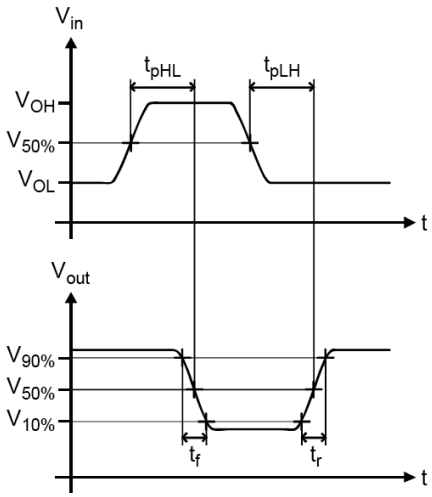
Definition of Delay Times



The propagation delay times are defined as the time delay between the 50% crossing of the input and the corresponding 50% crossing of the output.

The rise time and the fall time of the output signal are defined as the time required for the voltage to change from its 10% level to its 90% level (or vice versa).

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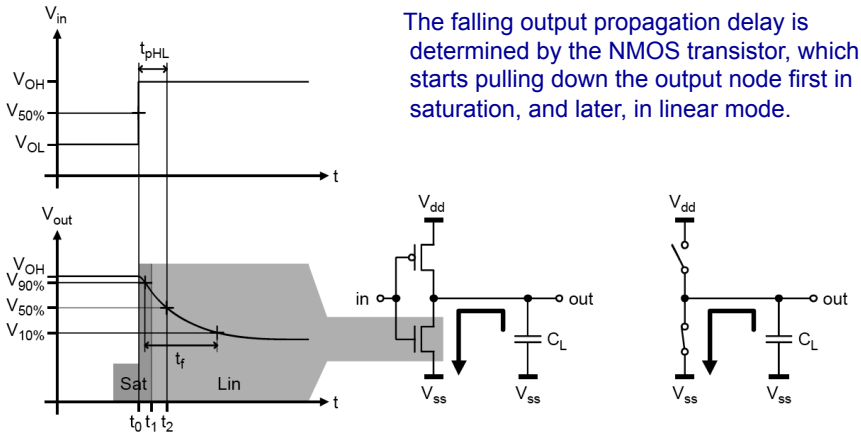
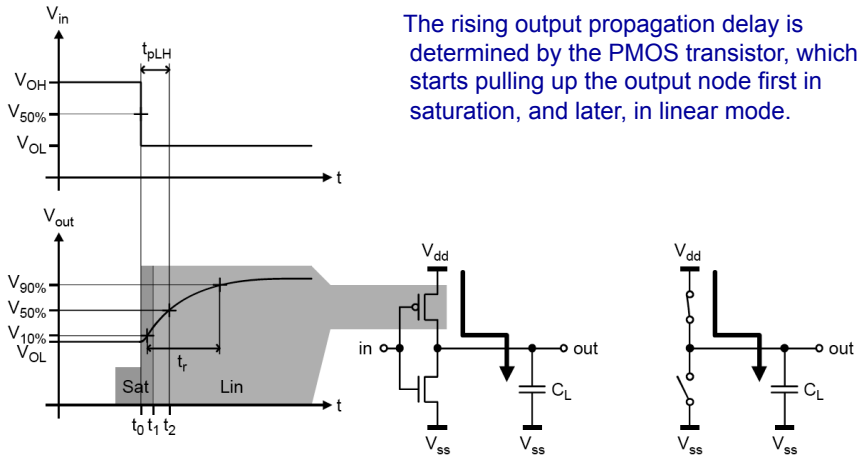
Calculation of Propagation Delays



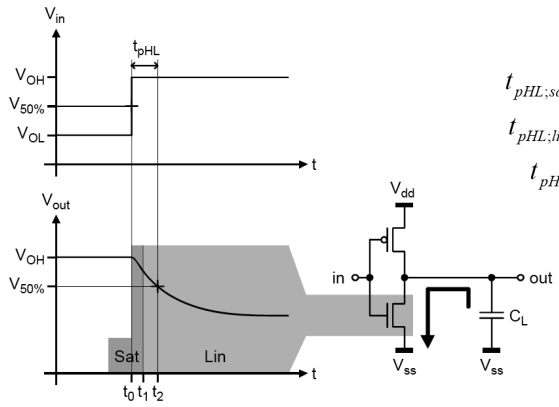
The falling output propagation delay is determined by the NMOS transistor, which starts pulling down the output node first in saturation, and later, in linear mode.

Calculation of Propagation Delays



The rising output propagation delay is determined by the PMOS transistor, which starts pulling up the output node first in saturation, and later, in linear mode.

Calculation of Propagation Delays



$$t_{pHL;sat} = t_1 - t_0$$

$$t_{pHL;lin} = t_2 - t_1$$

$$t_{pHL} = t_{pHL;sat} + t_{pHL;lin} = t_2 - t_0$$

$$i = C_L \frac{dV}{dt} \Leftrightarrow dt = C_L \frac{dV}{i}$$

The time required by the NMOS transistor in saturation and in linear region can be calculated separately.

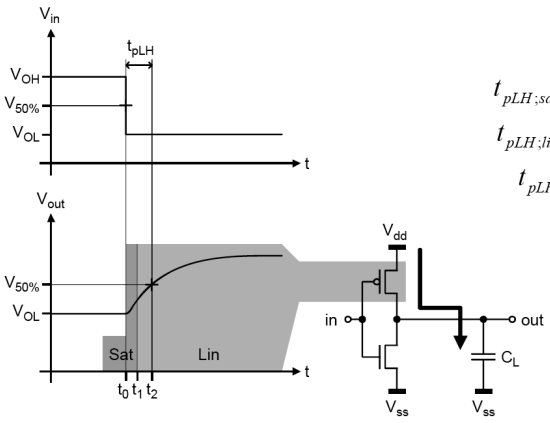
Calculation of Propagation Delays

$$t_{pHL;sat} = \frac{2nC_L V_{T0n}}{\beta_n (V_{OH} - V_{T0n})^2}$$

$$t_{pHL;lin} = \frac{nC_L}{\beta_n (V_{OH} - V_{T0n})} \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OL} + V_{OH}} - 1\right)$$

$$t_{pHL} = t_{pHL;sat} + t_{pHL;lin} = \frac{nC_L}{\beta_n (V_{OH} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OL} + V_{OH}} - 1\right)\right]$$

Calculation of Propagation Delays



$$t_{pLH;sat} = t_1 - t_0$$

$$t_{pLH;lin} = t_2 - t_1$$

$$t_{pLH} = t_{pLH;sat} + t_{pLH;lin} = t_2 - t_0$$

$$i = C_L \frac{dV}{dt} \Leftrightarrow dt = C_L \frac{dV}{i}$$

The time required by the PMOS transistor in saturation and in linear region can be calculated separately.

Calculation of Propagation Delays

$$t_{pLH;sat} = \frac{2nC_L V_{T0p}}{\beta_p (V_{dd} - V_{OL} - V_{T0p})^2}$$

$$t_{pLH;lin} = \frac{nC_L}{\beta_p (V_{dd} - V_{OL} - V_{T0p})} \ln\left(\frac{4(V_{dd} - V_{OL} - V_{T0p})}{2V_{dd} - V_{OL} - V_{OH}} - 1\right)$$

$$t_{pLH} = t_{pLH;sat} + t_{pLH;lin}$$

$$= \frac{nC_L}{\beta_p (V_{dd} - V_{OL} - V_{T0p})} \left[\frac{2V_{T0p}}{V_{dd} - V_{OL} - V_{T0p}} + \ln\left(\frac{4(V_{dd} - V_{OL} - V_{T0p})}{2V_{dd} - V_{OL} - V_{OH}} - 1\right)\right]$$

Calculation of Propagation Delays

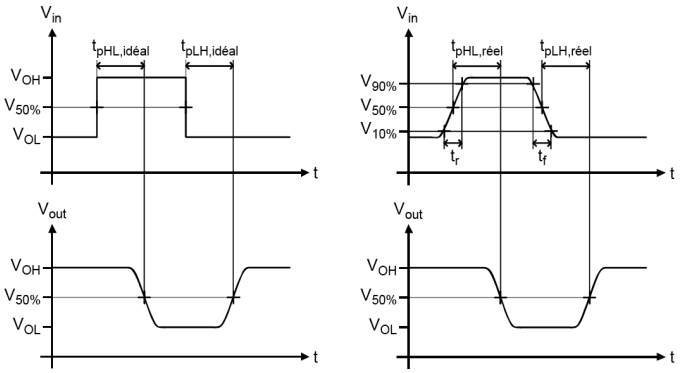
$$t_{pHL} = \frac{nC_L}{\beta_n (V_{OH} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OL} + V_{OH}} - 1 \right) \right]$$

$$t_{pLH} = \frac{nC_L}{\beta_p (V_{dd} - V_{OL} - V_{T0p})} \left[\frac{2V_{T0p}}{V_{dd} - V_{OL} - V_{T0p}} + \ln\left(\frac{4(V_{dd} - V_{OL} - V_{T0p})}{2V_{dd} - V_{OL} - V_{OH}} - 1 \right) \right]$$

Summary:

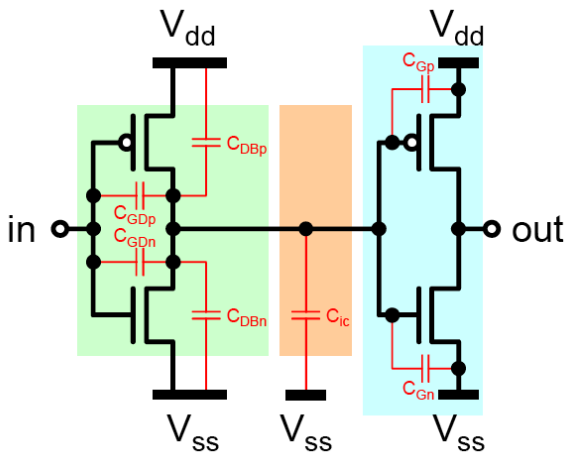
The propagation delay times are proportional to the load capacitance, and inversely proportional to the pull-up (or pull-down) transconductance.

Influence of Nonzero Input Rise/Fall Time



$$t_{pHL,réel} = \sqrt{t_{pHL,idéal}^2 + \left(\frac{t_r}{2}\right)^2} \qquad t_{pLH,réel} = \sqrt{t_{pLH,idéal}^2 + \left(\frac{t_f}{2}\right)^2}$$

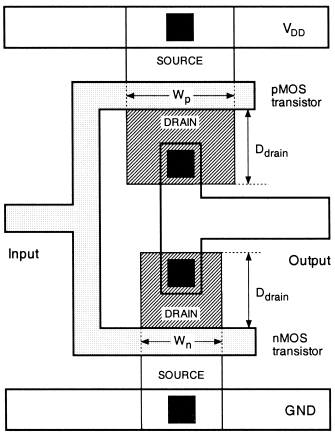
Components of the Output Load Capacitance



Increasing the Switching Speed

- Need to increase the amount of charge-up and charge-down current that switches the output.
- Increase the transistor (W/L) ratios both in the pull-up path and in the pull-down path.
- However: increasing transistor dimensions will influence the parasitic MOSFET capacitances.

- **The switching speed of a classical CMOS gate is ultimately limited by its intrinsic delay.**



Drain parasitics are mainly responsible for the intrinsic gate delay.

$$\begin{aligned} C_{load} &= C_{gd,n}(W_n) + C_{gd,p}(W_p) \\ &\quad + C_{db,n}(W_n) + C_{db,p}(W_p) \\ &\quad + C_{int} + C_g \\ &= f(W_n, W_p) \end{aligned}$$

A closer look at the typical CMOS inverter

Parasitic Capacitance Components

Drain parasitics:

$$C_{db,n} = W_n D_{drain} C_{j0,n} K_{eq,n} + 2(W_n + D_{drain}) C_{jsw,n} K_{eq,n}$$
$$C_{db,p} = W_p D_{drain} C_{j0,p} K_{eq,p} + 2(W_p + D_{drain}) C_{jsw,p} K_{eq,p}$$

Total capacitive load:

$$\begin{aligned} C_{load} &= (W_n C_{j0,n} K_{eq,n} + W_p C_{j0,p} K_{eq,p}) D_{drain} \\ &\quad + 2(W_n + D_{drain}) C_{jsw,n} K_{eq,n} \\ &\quad + 2(W_p + D_{drain}) C_{jsw,p} K_{eq,p} \\ &\quad + C_{int} + C_g \end{aligned}$$

Parasitic Capacitance Components

$$C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$$

$$\alpha_0 = 2D_{drain}(C_{jsw,n} K_{eq,n} + C_{jsw,p} K_{eq,p}) + C_{int} + C_g$$
$$\alpha_n = K_{eq,n}(C_{j0,n} D_{drain} + 2C_{jsw,n})$$
$$\alpha_p = K_{eq,p}(C_{j0,p} D_{drain} + 2C_{jsw,p})$$

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Propagation Delays

rising input
falling output

$$\tau_{PHL} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_n}\right) \times \left(\frac{L_n}{\mu_n C_{ox}(V_{DD} - V_{T,n})}\right) \times \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

falling input
rising output

$$\tau_{PLH} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_p}\right) \times \left(\frac{L_p}{\mu_p C_{ox}(V_{DD} - |V_{T,p}|)}\right) \times \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$

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Propagation Delays

rising input
falling output

$$\tau_{PHL} = \Gamma_n \left(\frac{\alpha_0 + (\alpha_n + R\alpha_p) W_n}{W_n} \right)$$

falling input
rising output

$$\tau_{PLH} = \Gamma_p \left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p \right) W_p}{W_p} \right)$$

Notice that with increasing transistor width W_n and W_p, both delays asymptotically approach fixed limit values, independent of external loads.

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Propagation Delays

$$\Gamma_n = \left(\frac{L_n}{\mu_n C_{ox} (V_{DD} - V_{T,n})} \right) \times \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$\Gamma_p = \left(\frac{L_p}{\mu_p C_{ox} (V_{DD} - |V_{T,p}|)} \right) \times \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

Intrinsic delay limits will decrease for

- Smaller gate length L
- Larger μ and C_{ox}

But for a given technology, the limits are fixed.

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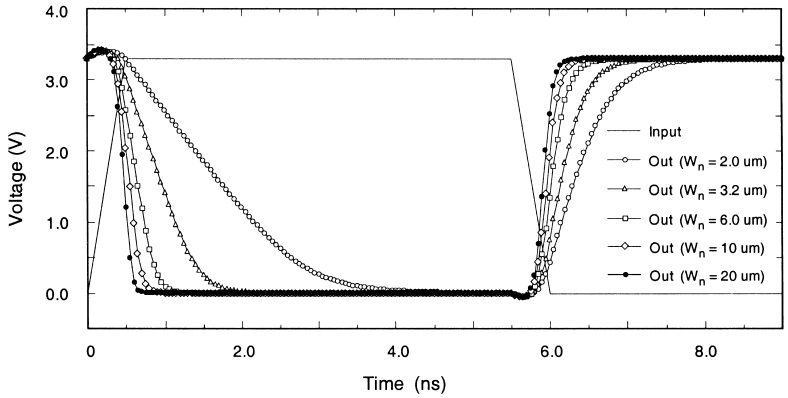
Improving propagation delay times by transistor sizing



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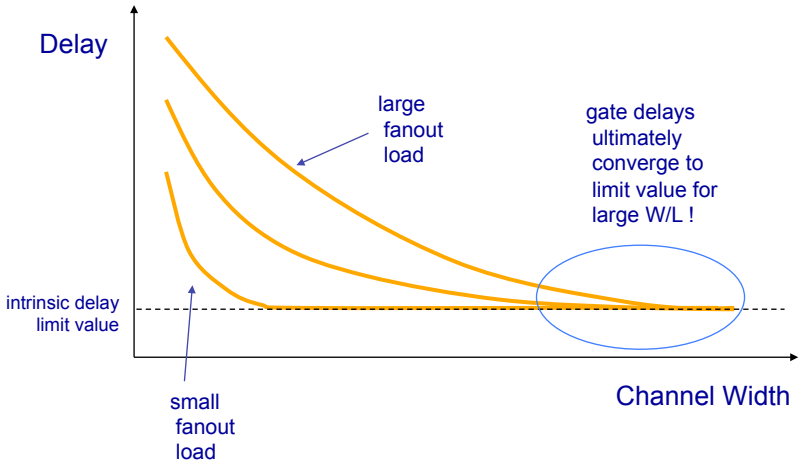
Improving propagation delay times by transistor sizing



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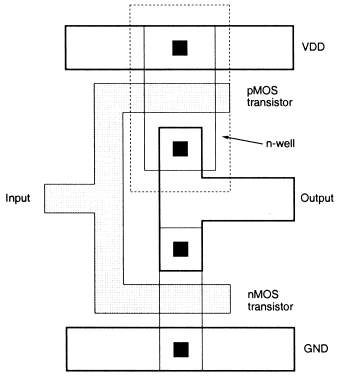
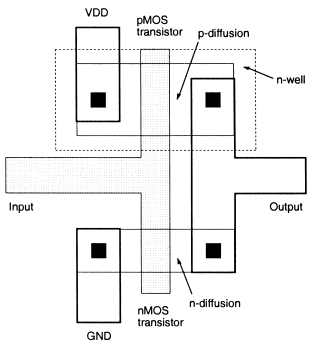
CMOS Inverter Layout





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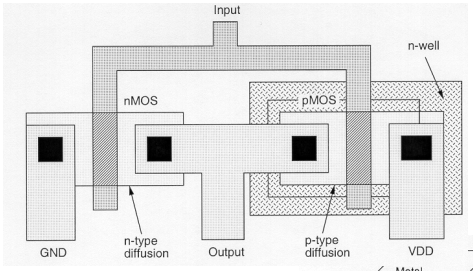
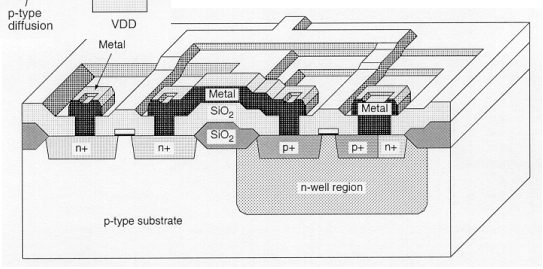
CMOS Inverter Layout



Mask layout of the inverter



Simplified cross-section

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