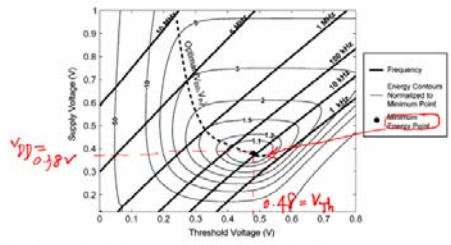
Subthreshold Circuit

THERE is significant research activity to minimize energy dissipation at the system level to lengthen battery lifetimes for embedded applications. Minimum energy analysis of CMOS circuits predicts the optimal operating point including clock frequencies, supply voltage, and threshold voltage. Our analysis shows that optimal supply voltage to minimize energy typically occurs in the subthreshold region. In order to investigate the optimal supply voltage, a new minimum energy design methodology is created to design circuits to operate at supply voltages far below the minimum energy point. The minimum energy design methodology was demonstrated on a fast Fourier transform (FFT) processor used for wireless sensor networks.

A distributed wireless sensor network is a collection of a large number (tens to thousands) of distributed microsensor nodes. Networked microsensors enable a variety of new applications such as warehouse inventory tracking, location sensing, machine-mounted sensing, patient monitoring, and building climate control [2]–[5]. The microsensor nodes must operate



Minimum energy point and constant energy and performance contours of the 16-b and 1024-pt FFT.

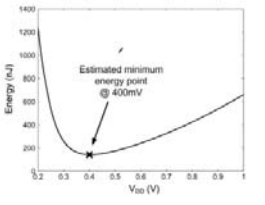


Fig. 4. Estimated minimum energy point for the FFT using a typical transistor in a 0.18-μm technology occurs at 400 mV which is lower than the threshold voltage (450 mV).

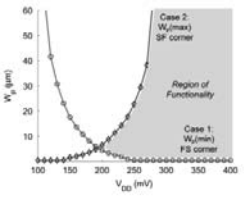


Fig. 5. Minimum voltage operation of the inverter is affected by process variations. Given the worst case corners, Fast NMOS/Slow PMOS (FS) and Slow NMOS/Fast PMOS (SF), the minimum voltage occurs at 195 mV.

XOR

A 0 1 1
B 0 1 0
Z 0 1 1 0

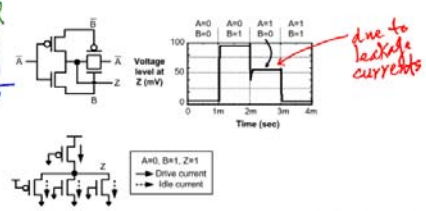


Fig. 6. Tiny XOR gate illustrates the effect of parallel leakage. The idle current through the three parallel devices degrades I_{on}/I_{off} and affects functionality for $A = 1$ and $B \approx 0$.

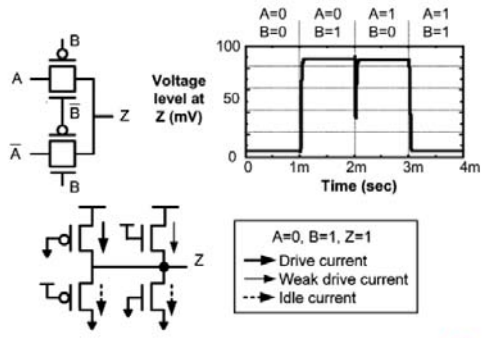


Fig. 7. A transmission gate XOR has balanced leakage and is functional for all input vectors at 100 mV.

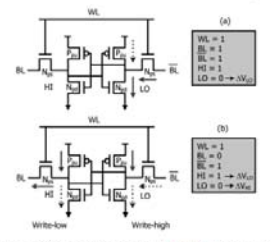


Fig. 8. The read and write conditions places sizing constraints on the memory cell. They are analyzed at the worst case process corners to account for large subthreshold leakage currents.

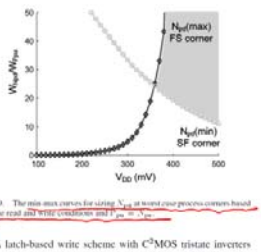
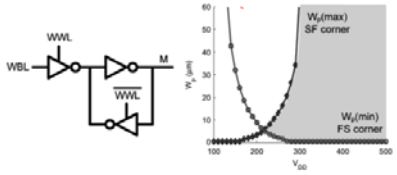


Fig. 9. The min-max curves for sizing N_{pn} at worst case process corners based on the read and write conditions and $P_{pn} = N_{pn}$.

A latch-based write scheme with C^2MOS tristate inverters is a more robust design for subthreshold operation (Fig. 10). Analysis of the latch-based write scheme is performed at the



Latch-based write access is analyzed at the worst case process corners.

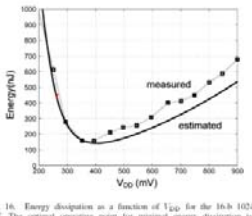


Fig. 16. Energy dissipation as a function of V_{DD} for the 16-b 1024-pt FFT. The optimal operating point for minimal energy dissipation is at V_{DD} = 370 mV.

The figure shows that our energy contour estimation technique predicts leakage energy well, but not switching energy. The energy is measured for the clock frequencies specified in Fig. 17.

Fig. 18 shows the energy dissipated for all operating points. The minimum energy point occurs at 350 mV for the 16-b processor and is at 400 mV for the 8-b processor. Eight-bit processing has a lower activity factor which reduces the ratio of switching energy to leakage energy. Thus, the optimum point is shifted toward larger minimum supply voltage [15]. At the optimal operating points for both 8-b and 16-b processing, the