THERE is significant research activity to minimize energy dissipation at the system level to lengthen battery lifetimes for embedded applications. Minimum energy analysis of CMOS circuits predicts the optimal operating point including clock frequencies, supply voltage, and threshold voltage. Our analysis shows that optimal supply voltage to minimize energy typically occurs in the subthreshold region in order to investigate the optimal supply voltage, a new minimum energy design methodology is created to design circuits to operate at supply voltages far below the minimum energy point. The minimum energy design methodology was demonstrated on a fast Fourier transform (FFT) processor used for wireless sensor networks.

A distributed wireless sensor network is a collection of a large number (tens to thousands) of distributed microsensor nodes. Networked microsensor enable a variety of new applications such as warehouse inventory tracking, location sensing, machine-mounted sensing, patient monitoring, and building climate control [3]-[5]. The microsensor nodes must operate...
The figure shows that our energy consumption estimation technique predicts leakage energy well, but not switching energy. The leakage is measured for the clock frequencies specified in Fig. 1. The minimum energy point occurs at 200 MHz for the 1.6 V processor and is at 350 MHz for the 1.8 V processor. Higher frequencies have lower activity factor which reduces the ratio of switching energy to leakage energy. Thus, the optimum point is shifted toward larger minimum supply voltage (VDD). As the selection interval increases, the best 1.6 and 1.8 measurements are