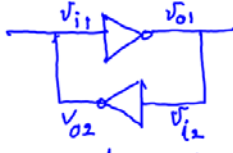


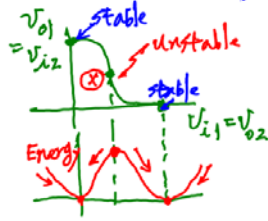
EE 222 Lecture 5 Jan 23, 2017

Bistable latch

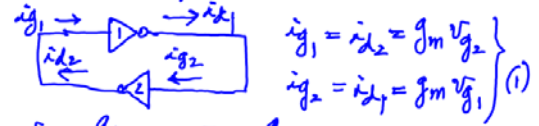


Two stable points

$(V_{i1} = V_{o2} = V_{DD}, V_{o1} = V_{i2} = 0)$
 $\& (V_{i1} = V_{o2} = 0, V_{o1} = V_{i2} = V_{DD})$
 The point where $V_{i1} (= V_{o2}) = V_{o1} (= V_{i2})$ is unstable



Small signal analysis at \otimes .



$$v_{g1} = \frac{q_1}{C_g} \quad v_{g2} = \frac{q_2}{C_g} \quad \dots \dots \dots (2)$$

$$\text{also } \left. \begin{aligned} i_{g1} &= C_g \frac{dv_{g1}}{dt} \\ i_{g2} &= C_g \frac{dv_{g2}}{dt} \end{aligned} \right\} \dots \dots \dots (3)$$

$$\text{From (1) \& (3) } \left. \begin{aligned} g_m v_{g2} &= C_g \frac{dv_{g1}}{dt} \\ g_m v_{g1} &= C_g \frac{dv_{g2}}{dt} \end{aligned} \right\} \dots \dots \dots (4)$$

From (4)

$$g_m v_{g2} = C_g \frac{dv_{g1}}{dt} = C_g \frac{d}{dt} \left(\frac{C_g}{g_m} \frac{dv_{g2}}{dt} \right)$$

$$g_m v_{g2} = \frac{C_g^2}{g_m} \frac{d^2 v_{g2}}{dt^2}$$

$$\frac{d^2 v_{g2}}{dt^2} - \left(\frac{g_m}{C_g} \right)^2 v_{g2} = 0$$

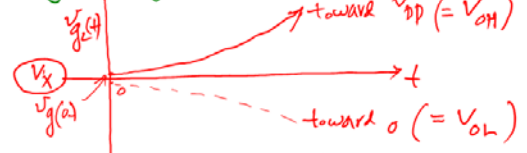
let $\frac{1}{\tau} = \frac{g_m}{C_g}$, then $\frac{d^2 v_{g2}}{dt^2} - \frac{1}{\tau^2} v_{g2} = 0$

solving for v_{g2} by Laplace transformation

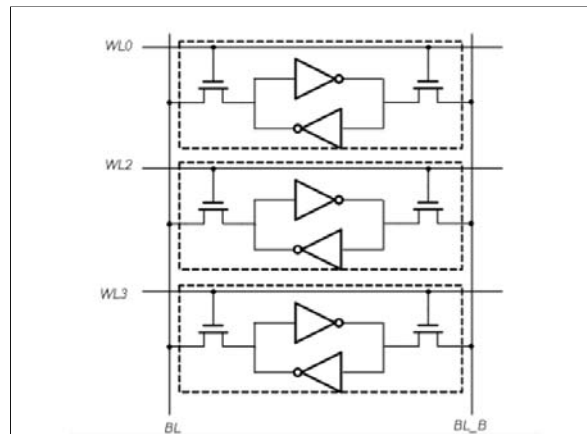
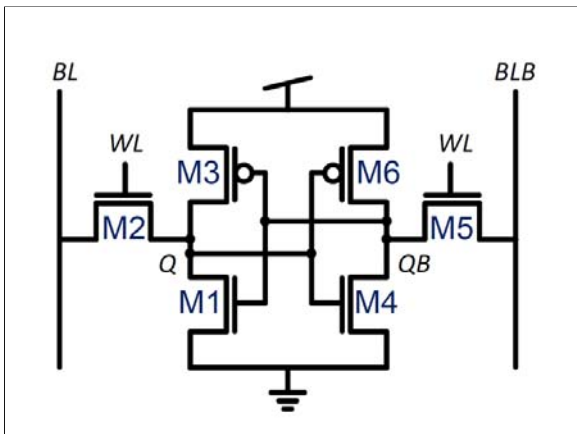
$$s^2 v_{g2}(s) - s v_{g2}(0) - v_{g2}'(0) - \left(\frac{1}{\tau} \right)^2 v_{g2}(s) = 0$$

$$\text{For } v_{g2}(0) = 0 \quad v_{g2}'(0) = 0 \quad v_{g2}(s) = \frac{s v_{g2}(0)}{s^2 - \left(\frac{1}{\tau} \right)^2} = \frac{1}{2} v_{g2}(0) \left[\frac{1}{s + \frac{1}{\tau}} + \frac{1}{s - \frac{1}{\tau}} \right]$$

$$\Rightarrow v_{g2}(t) = \frac{1}{2} v_{g2}(0) \left(e^{-t/\tau} + e^{+t/\tau} \right)$$



thus \otimes is an unstable point
 any perturbation will lead to migration
 to a stable point (V_{OH} or V_{OL})



Two sides of the bitcell

- Share Horizontal Routing (WWL).
- Share Vertical Routing (BL, BLB).
- Share Power and Ground.
- Word line routed double on Poly and Metal (reduce resistance)

CMOS Performance Optimization

- Sizing: Optimal performance with equal fan-out per stage
- Extendable to general logic cones through "logical effort"
- Equal effective fan-outs ($\rho C_{in}/C_i$) per stage
- Example: memory decoder

(Ref: I. Sutherland, Morgan-Kaufmann)

Slide 3.38
This philosophy is best reflected in the popular "logical effort"-based design optimization methodology. The delay of a circuit is minimized if the "effective fan-out" of each stage is made equal (and set to a value of approximately 4). Though this technique is very powerful, it also guarantees that power consumption is maximized. In the coming chapters, we will reformulate the logical-effort methodology to bring power into the equation.

* Logical Effort: Designing Fast CMOS Circuits
by Ivan Sutherland, David Sproat, David Harris
Morgan Kaufmann Publishers, 1999

Power Minimization

$$P = C V_{DD} \Delta V_{swing} f_{clock}$$

$$P = \bar{F} C V_{DD}^2 f_{clock}$$

For a given f_{clock} ,

$$P = V_{DD} \cdot I \quad I = \frac{C \Delta V}{T} = C \Delta V f_{clock}$$

$$\min P = C V_{DD}^2 f_{clock}$$

subject to delay $<$ delay specification

\Rightarrow reduce C , V_{DD} (big influence)

delay $\propto \frac{C V_{DD}}{W}$, $C = f(W \text{ (tr. size), interconnect})$

Increasing W reduces delay, but increase C , thus P .

Sub-threshold SRAM

Sub- V_{TH} operation demonstrated in 65 nm memory chip

Chip functions without error to below 400 mV, holds without error to below 260 mV

- At 400 mV, 3.28 mW and 475 kHz at 27°C
- Reads to 320 mV (27°C) and 360 mV (85°C)
- Writes to 380 mV (27°C) and 350 mV (85°C)

(Ref: B. Gelsman, ISSCC'06)

Slide 11.28
A 256 kb SRAM memory was designed and tested using the cell of the previous slide. Reliable operation down to 400 mV was demonstrated. Though this represents great progress, it is clear that addressing further voltage scaling of SRAMs (or any other memory type) is essential if ultra low power design is to be successful. (sorry if this starts to sound like a broken record!)

Importance of Low-Level Analysis

$R \propto T \uparrow$

when an delays (one at higher temperature) can cause malfunction of a latch!
latch 0 instead of 1!