Bistable latch

\[ V_{I1} = V_{O1} = V_{PP}, \quad V_{O1} = \bar{V}_{X} = 0 \]

\[ V_{I2} = V_{O2} = V_{SS}, \quad V_{O2} = \bar{V}_{X} = 0 \]

The point where \( V_{I1} (V_{O2}) = V_{I2} (V_{O1}) \) is unstable

Small signal analysis at \( \Theta \).

\[ \frac{dV_I}{dV_O} = \frac{gm_{I1}}{gm_{O1}} \]

\[ \frac{dV_O}{dV_I} = \frac{gm_{O1}}{gm_{I1}} \]

\[ V_{I1} = \frac{g_m}{g_{m1}} \quad V_{O1} = \frac{g_m}{g_{m1}} \]

Also \[ V_{I2} = \frac{g_m}{g_{m2}} \quad V_{O2} = \frac{g_m}{g_{m2}} \]

From (1) and (2) \[ \frac{gm_{O1}}{gm_{I1}} = \frac{g_m}{g_{m1}} \]

Thus \( \Theta \) is an unstable point. Any perturbation will lead to migration to a stable point (\( \bar{V}_{X} \) or \( V_{X} \)).
Two sides of the bitcell
- Share Horizontal Routing (W, W′),
- Share Vertical Routing (BL, BLB),
- Share Power and Ground,
- Word line routed double on Poly and Metal (reduce resistance)

Power Minimization

\[ P = C \frac{V_{DD}}{2} \times V_{DD} \times f_{\text{clock}} \]

For a given \( f_{\text{clock}} \),

\[ \min P = C \frac{V_{DD}^2}{2} f_{\text{clock}} \]

subject to delay < delay specification

\[ \Rightarrow \text{reduce } C, \frac{V_{DD}}{2} \text{ (big influence)} \]

\[ \text{delay} \propto \frac{V_{DD}}{2} \left( \frac{1}{C} \right) \text{ (intrinsic)} \]

\[ \text{increased } V_{DD} \text{ reduces delay, but increases } C \text{ thus } P \]

Importance of Low-Level Analysis

Clock

Data

Latch

Clock

Data

Latch

Clock

Data

Latch

Whether delays occur at high temperature

Latch 0 instead of 1!