VLSI Design – I

Interconnect Parasitics

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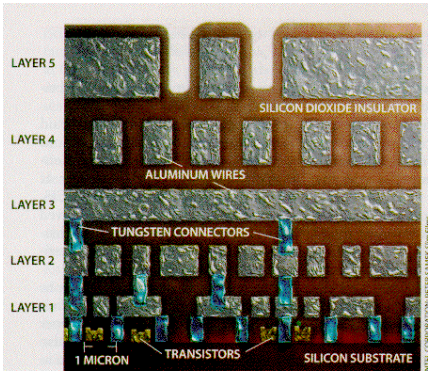
Interconnect Delay

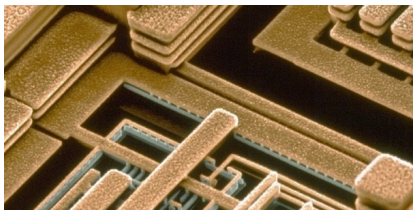
- In deep submicron CMOS technologies, the delay due to interconnect parasitic capacitances and resistances dominates the signal propagation.
- Need a detailed understanding of the interconnect parasitic effects !

Interconnect Modeling for High Speed



In the following, we will focus on modeling of high-speed behavior for interconnect lines:

- Capacitance / inductance
- Coupling effects
- Cross-talk…



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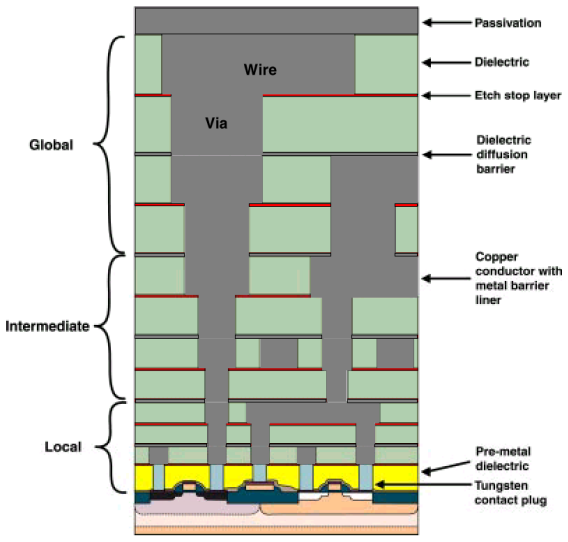
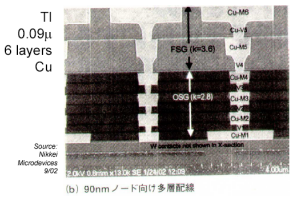
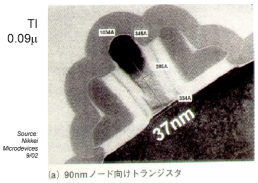
Typical Chip Cross Section



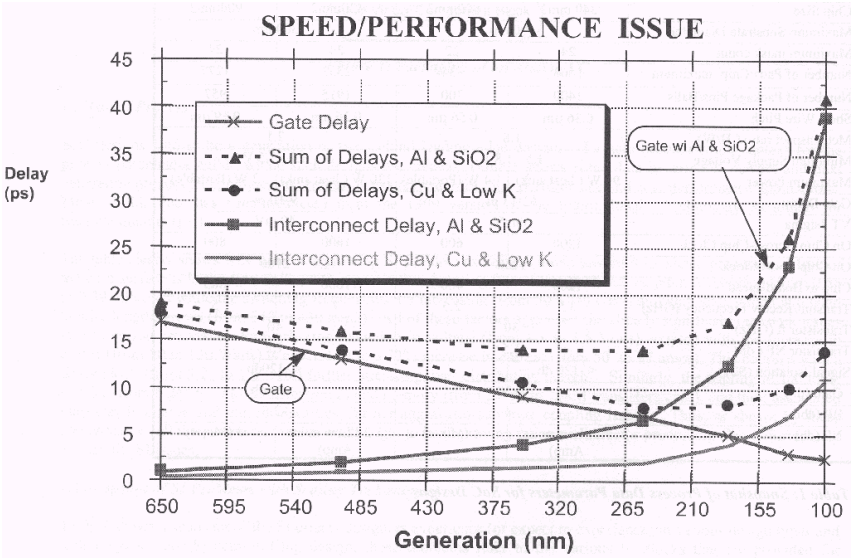


(b) 90nmノード向け多層配線



(a) 90nmノード向けトランジスタ

LSM



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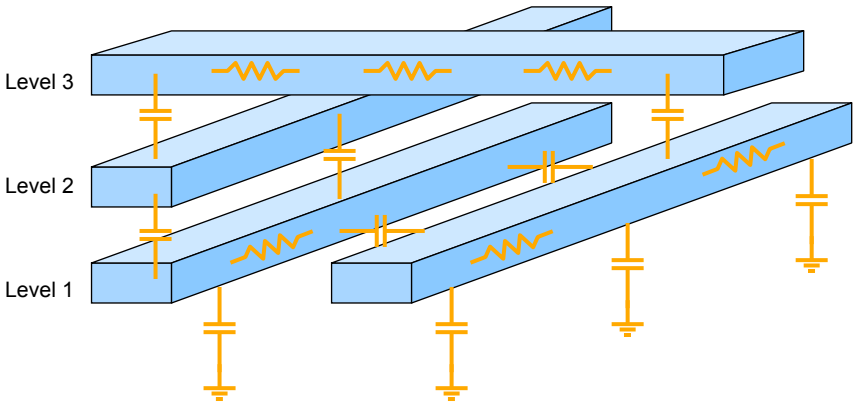
Typical Multi-Level Interconnect



Series resistances of wire segments + **Coupling capacitances between wire segments** + **Ground caps**

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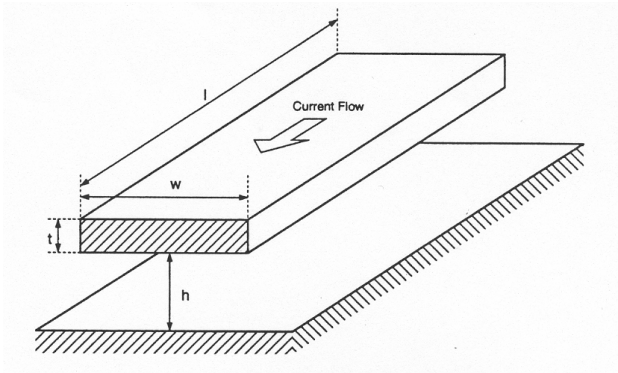

Cross-section of a single wire over ground-plane

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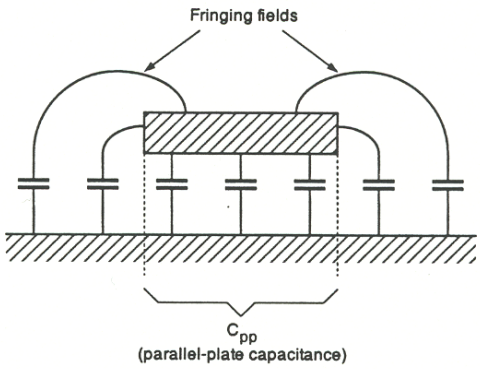

Parallel-plate and fringing-field capacitances

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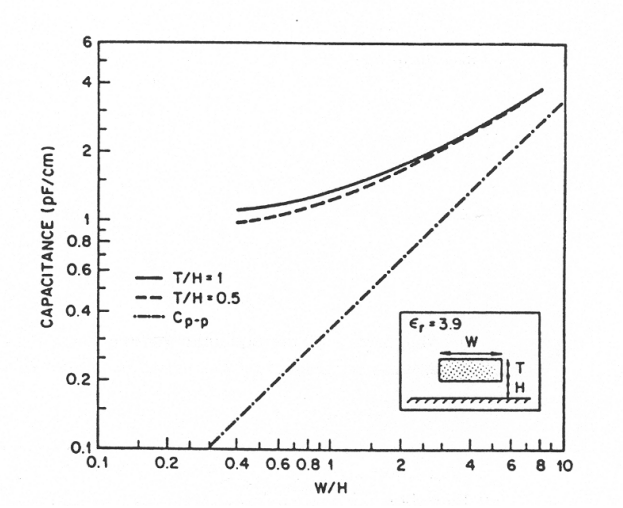
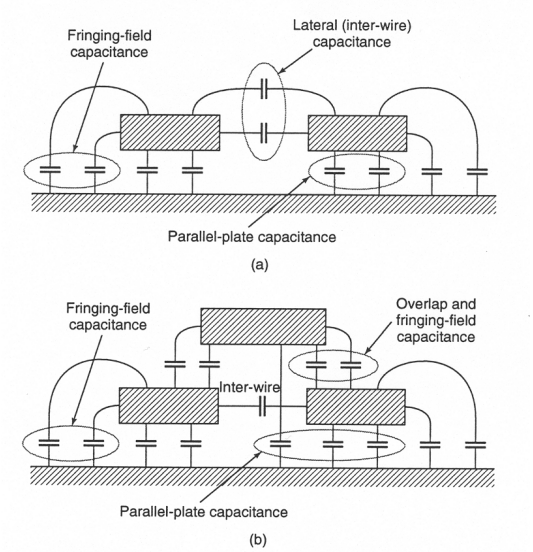
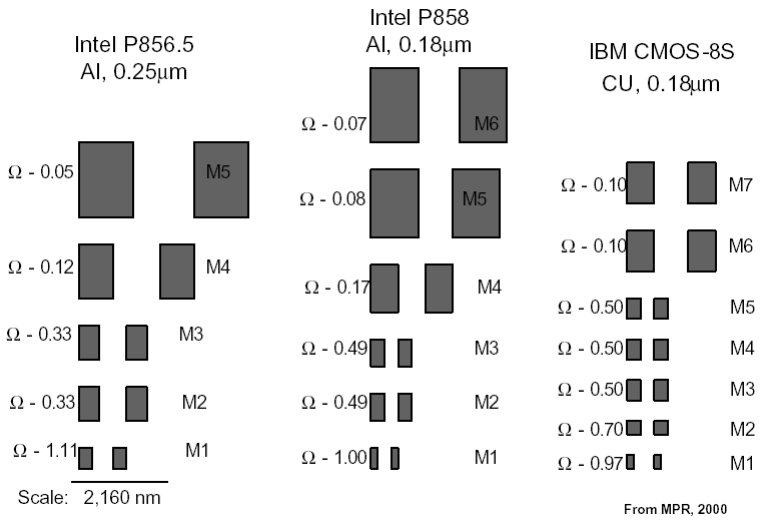


Influence of fringing field capacitance



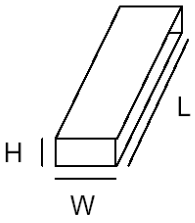


	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54				pp in aF/µm^2		
Al1	30	41	57		fringe in aF/µm		
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

	Poly	Al1	Al2	Al3	Al4	Al5
Interwire Cap	40	95	85	85	85	115

per unit wire length in aF/µm for minimally-spaced wires

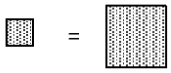
Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho}{H} \cdot \frac{L}{W}$$

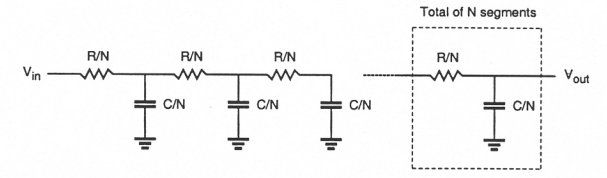
Sheet Resistance $R_{\square}$

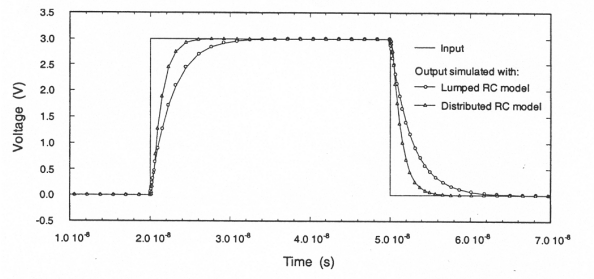
$R_1 = R_2$



Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

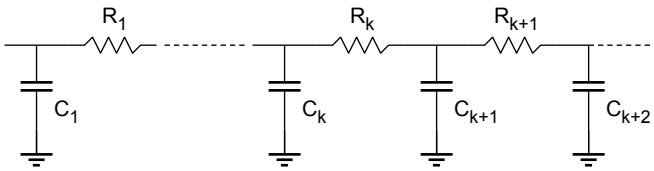
Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1





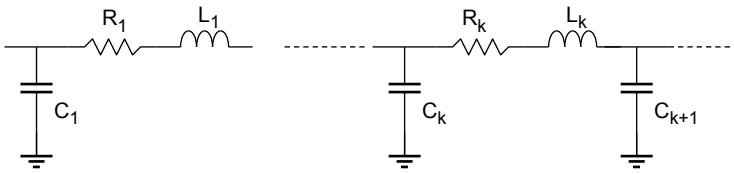
Distributed RC delay modeling

Distributed RC Model



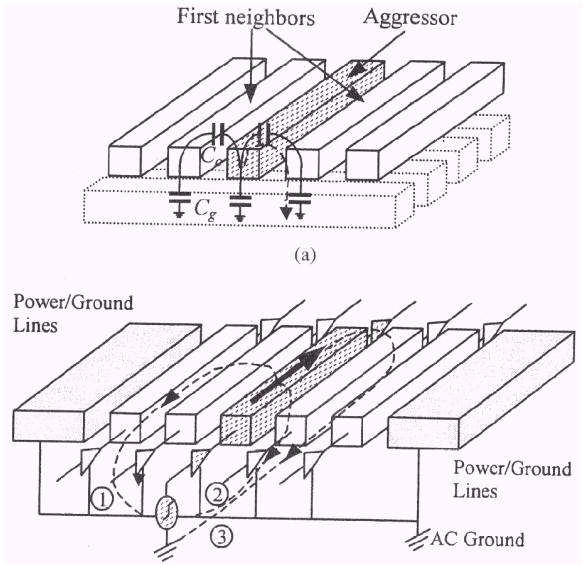
- For slow signals and/or short wire segments, distributed RC model (including capacitive coupling to neighboring wires) will provide a sufficiently accurate picture.
- Several precise (albeit computationally costly) methods exist for the extraction of R and C values.
- Delays and coupling effects can be simulated using the RC model.

Distributed RLC Model



- However: Self and mutual inductance of a wire segment must also be considered if the signal rise / fall times are on the same order of magnitude as the time-of-flight.
- Longer wire lengths, faster switching times and low resistance (copper) interconnects are becoming very common in VDSM technologies.

  → Increasing importance of inductance effects.



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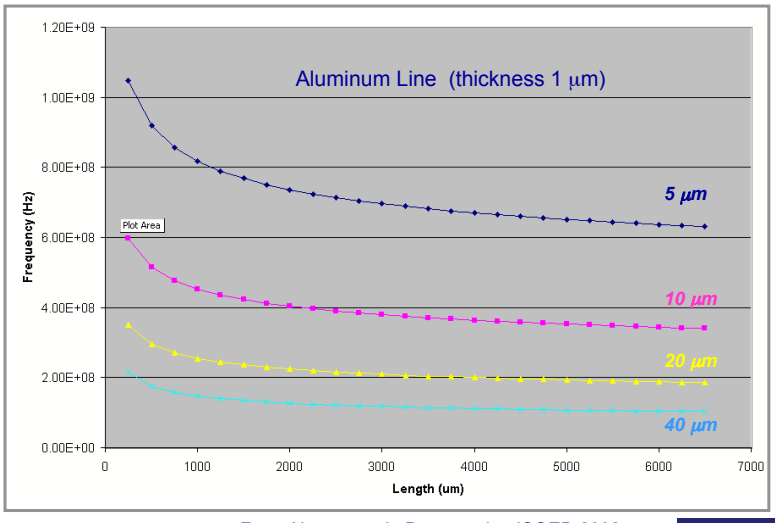
Maximum Frequency at Which One Can Ignore Inductive Effects in a Wire



From Akcasu et al. Presented at ISQED 2002

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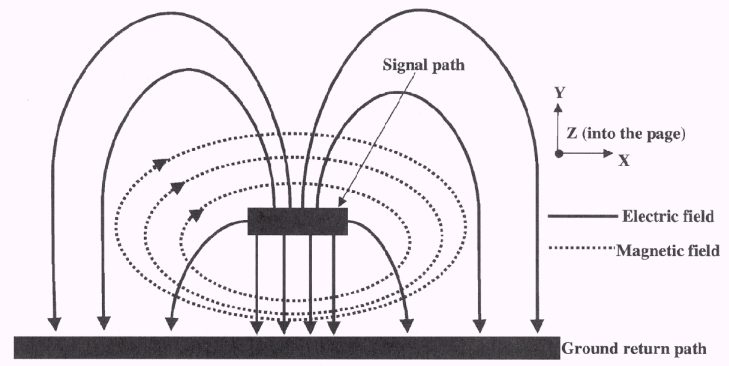
Electric and Magnetic Fields Associated with a Signal Wire



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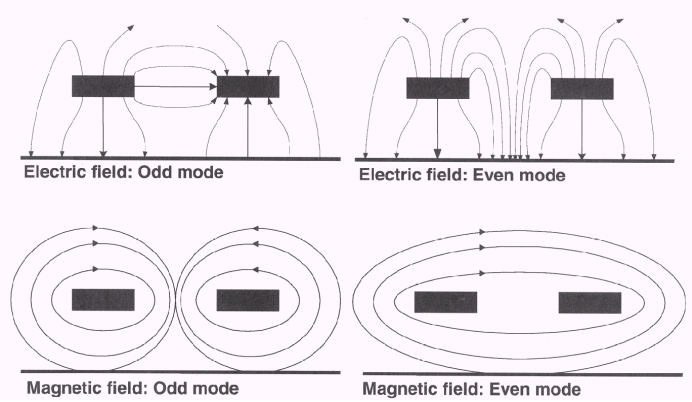
Electric and Magnetic Fields Associated with Two Parallel Wires



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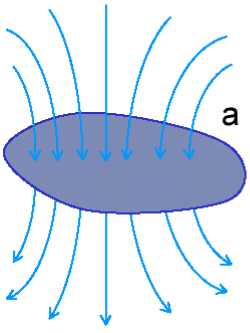
Calculation of Wire Inductances

Start with Maxwell's Equations

$$\nabla \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t}$$
$$\nabla \times \boldsymbol{H} = \frac{\partial \boldsymbol{D}}{\partial t} + \boldsymbol{J}$$
$$\nabla \bullet \boldsymbol{B} = 0$$
$$\nabla \bullet \boldsymbol{D} = \rho$$

Calculation of Wire Inductances

Flux Φ_a is the integral of the magnetic field over the area enclosed by a conductor loop



Change of Flux creates Voltage (Faraday's Law)

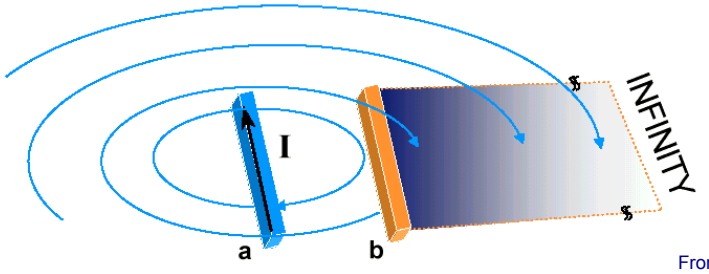
$$V_a = \frac{d}{dt}\Phi_a$$

$$\Phi_a = L_{aa} I_a$$

From Pileggi et al. DAC 2001

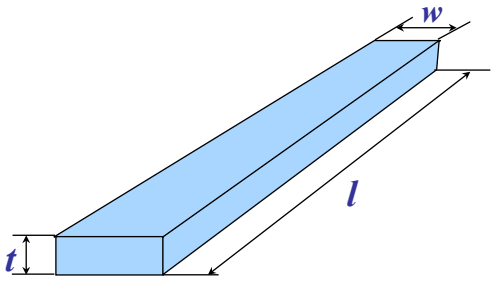
Calculation of Wire Inductances

- Flux through own virtual loop defines partial self inductance of active segment
- Flux through other virtual loop defines partial mutual inductance between segments



From Pileggi et al. DAC 2001

Calculation of Wire Inductances



$$L(\mu H) = 0.002l\left\{\ln\left[\frac{2l}{(w+t)}\right] + 0.5 - k\right\}$$

Where $k = f(w,t)$

$0 < k < 0.0025$

l,t,w *in cm*

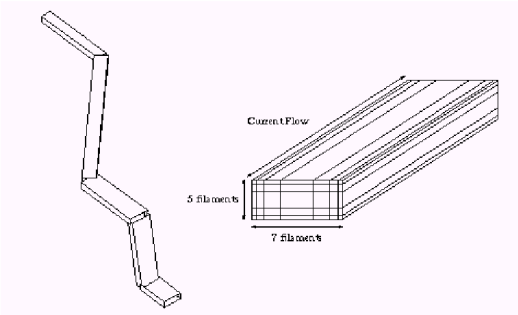
$$R(\Omega) = \frac{\delta l}{(w\ t)}$$

$$Z(j\omega) = R + j\omega L \quad \text{Where} \quad \omega = 2\pi f$$

From Akcasu et al. ISQED 2002

Calculation of Wire Inductances

Partial Inductance calculation of an interconnect divided into multiple segments, each of which is a bundle of multiple filaments:

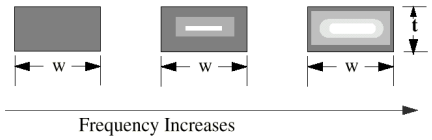


$$L_{ij} = \sum_{k=1}^{K} \sum_{m=1}^{M} \frac{\mu}{4\pi a_k a_m} \frac{1}{b_k} \int_{a_k}^{c_k} \int_{b_m}^{c_m} \int_{a_m} \frac{dl_k \bullet dl_m}{r_{km}} da_k da_m$$

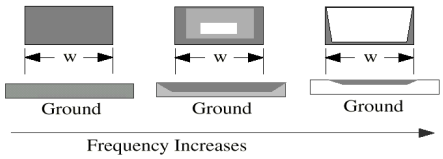
From S. Lin
ASIC/SOC 2000

Influence of Skin Effect at High Frequencies

Current distribution versus frequency in an isolated conductor:

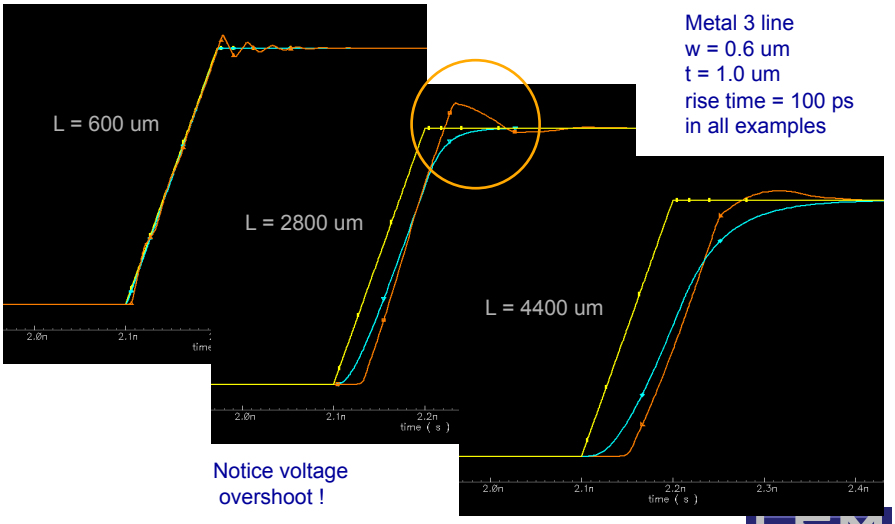


Current distribution versus frequency in a conductor over a ground plane:



From S. Lin
ASIC/SOC 2000

Self Inductance Effect on a Single Wire



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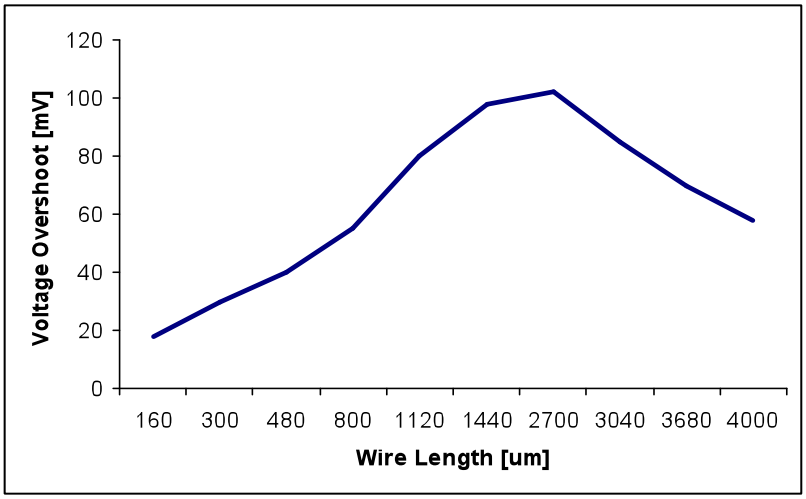
Voltage Overshoot Due to Inductance



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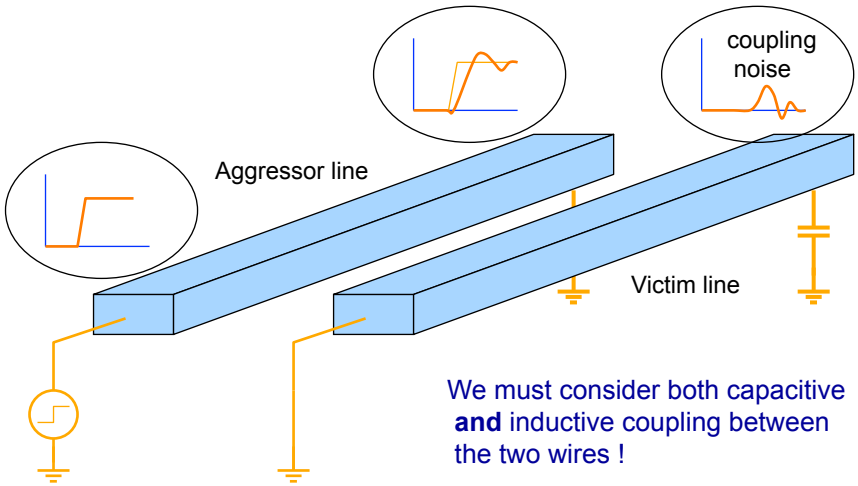
Coupling Between Two Parallel Adjacent Wires



We must consider both capacitive **and** inductive coupling between the two wires !

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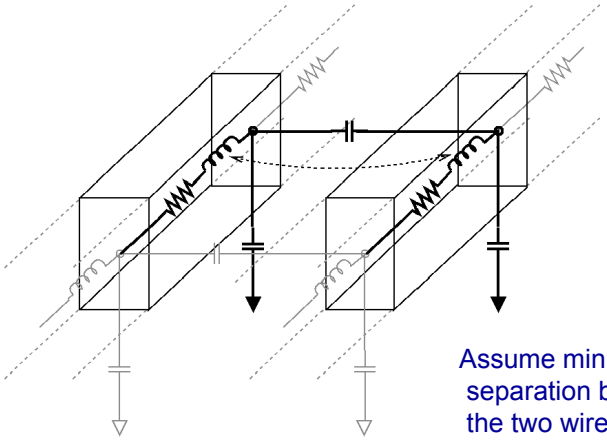
Partial RLCM model of Two Adjacent Wires



Assume minimum separation between the two wires.

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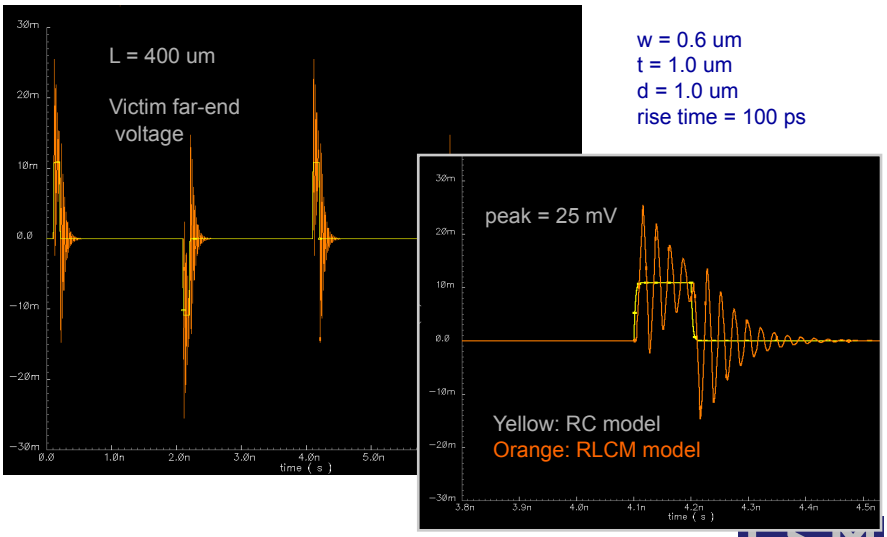
Coupling Between Two Parallel Adjacent Wires



w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

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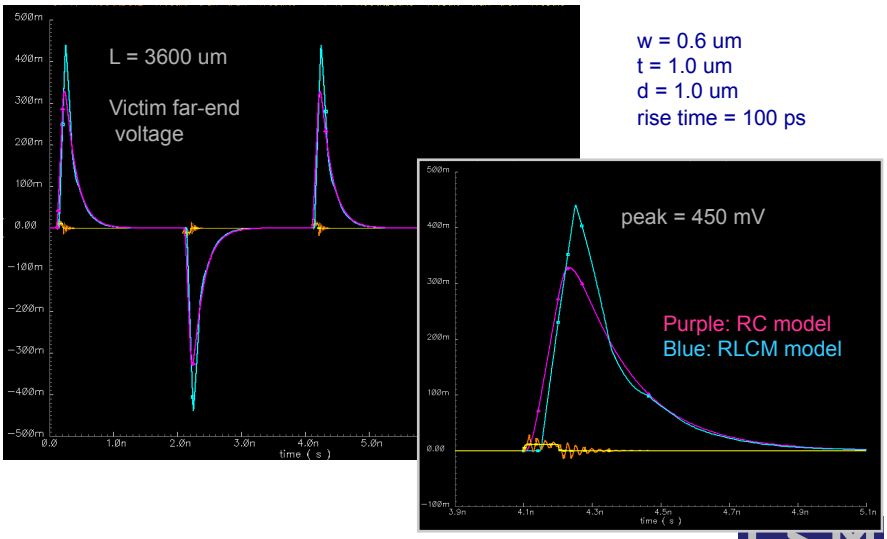
Coupling Between Two Parallel Adjacent Wires



w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

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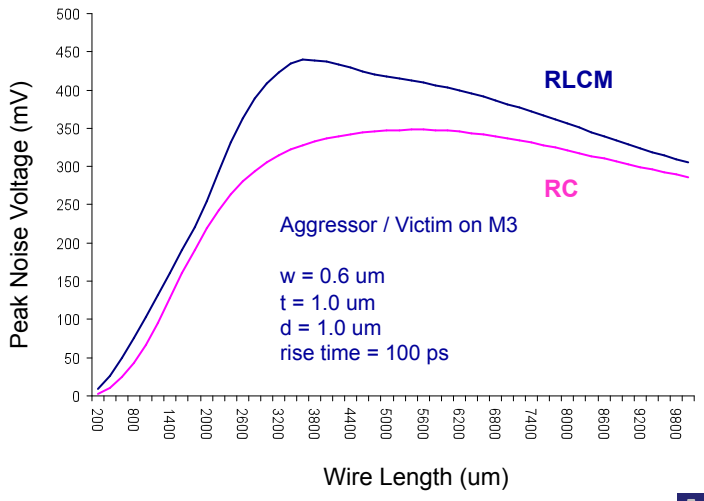
Coupling Noise on Victim Line



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Techniques for Reducing Crosstalk

- **Increasing signal line width**
  - **Increases signal-to-ground capacitance compared to signal-to-signal capacitance**
- **Increase spacing between signals**
  - **Decreases capacitive coupling**
  - **Can increase inductive coupling (larger loops)**
- **Shielding signals with power and ground**
  - **Provides known low-impedance return paths**
- **Buffer insertion**
  - **Decrease line lengths, stagger buffers**
- **Differential signal lines**
  - **Can be very effective for high-speed signals**

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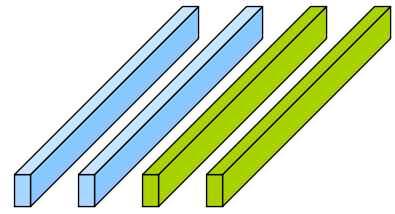
Differential Signal Lines



differential aggressor pair

differential victim pair

Consider two adjacent **differential** line pairs, one acting as the aggressor and the other as the victim.

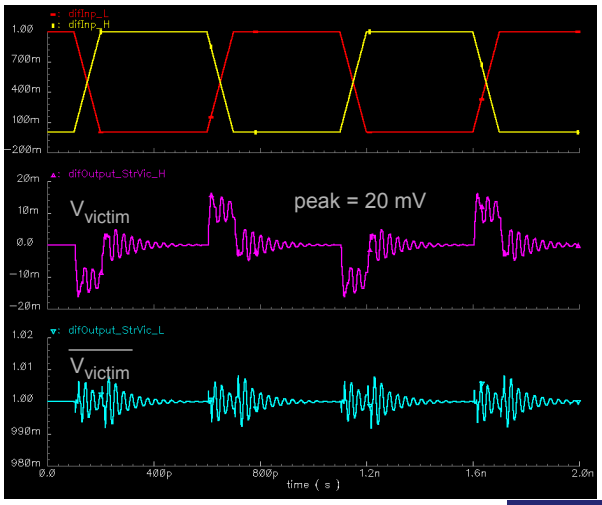
All lines have the same amount of capacitance to the ground plane.

Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

L = 400 um

Victim far-end voltages (individual)

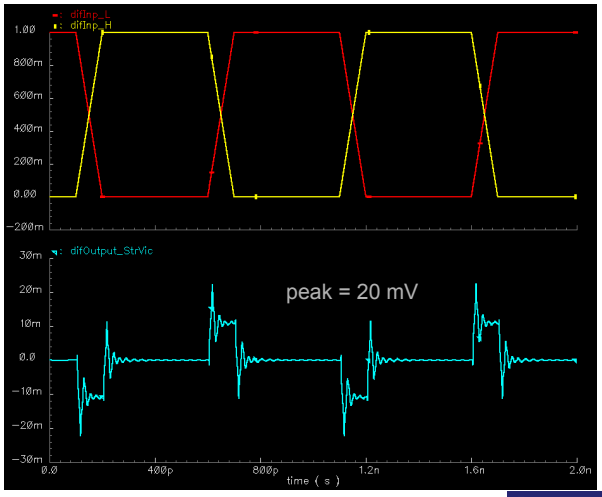


Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

L = 400 um

Victim far-end
voltage
(differential)

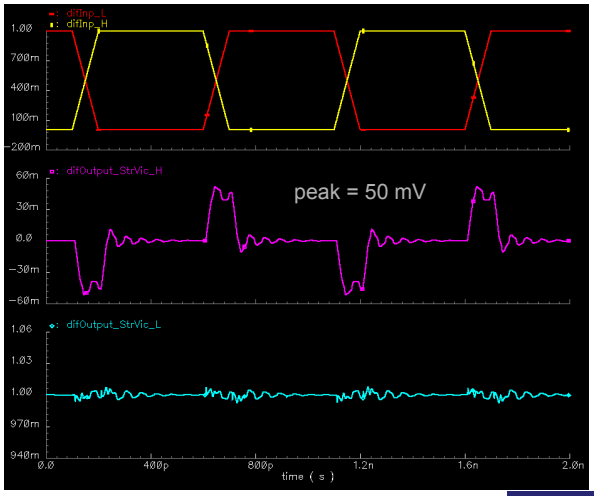


Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

L = 800 um

Victim far-end
voltages
(individual)

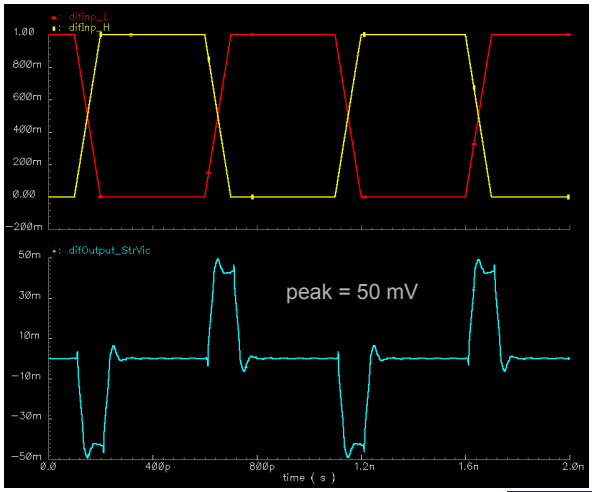


Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

L = 800 um

Victim far-end voltage (differential)



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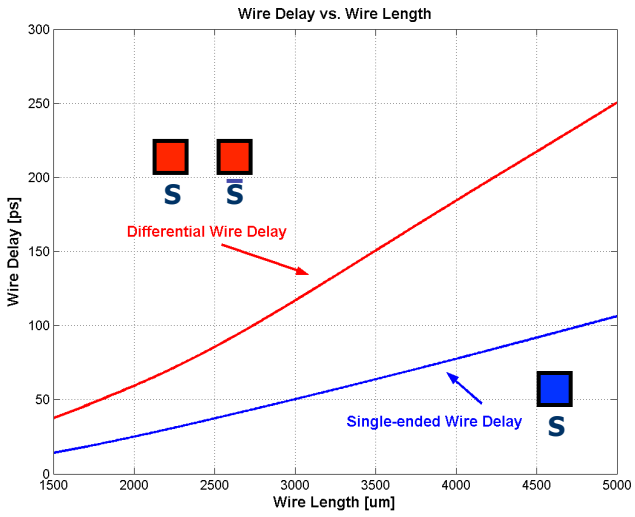
Delay in Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps



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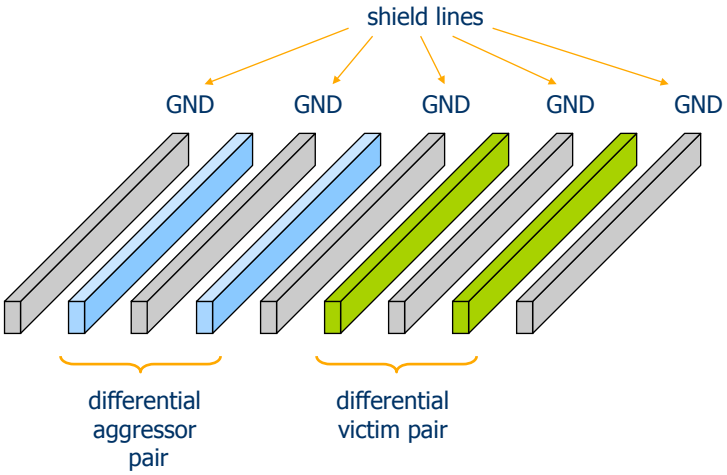
Shielded Differential Signal Lines



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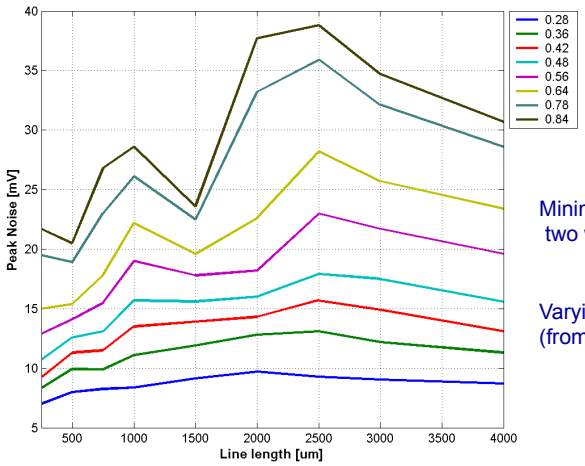
Shielded Differential Signal Lines



Minimum spacing between two wires s = 0.28 um

Varying wire width (from 0.28 um to 0.84 um)

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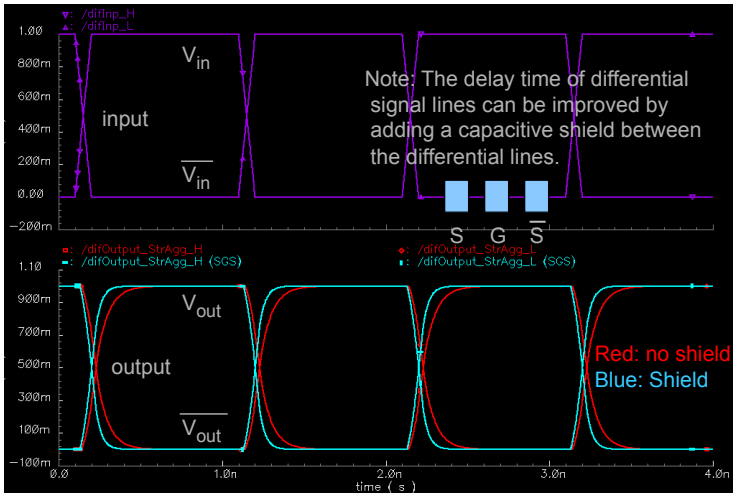
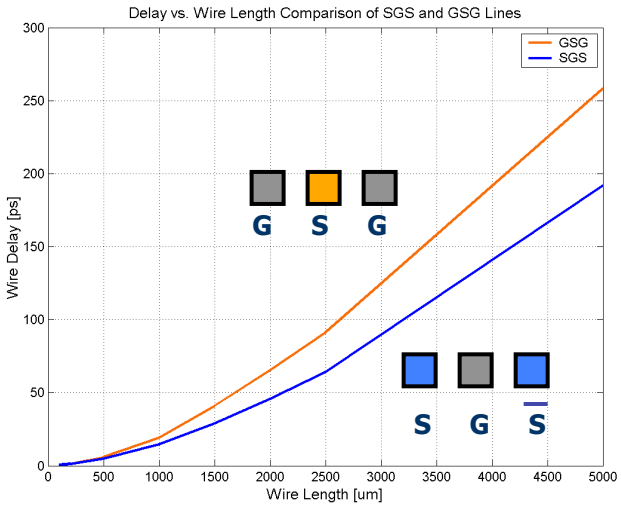
Shielded Differential Signal Lines



Shielded Differential Signal Lines

Metal 3 line
w = 0.6 um
t = 1.0 um
rise time = 100 ps
in all examples



Twisted Differential Signal Lines

- To further improve coupling noise immunity, consider twisting each differential line at regular intervals.
- Twisting (transposition) points of adjacent differential line pairs should not overlap with each other.

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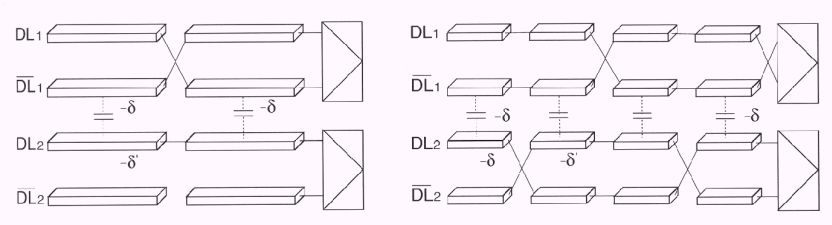
Twisted Differential Signal Lines



This technique is mainly used for data lines in memory arrays, to reduce and/or eliminate **capacitive** coupling.

However, it is also very effective for eliminating **inductive** coupling between differential signal lines.

From K. Itoh
Springer Verlag 2001

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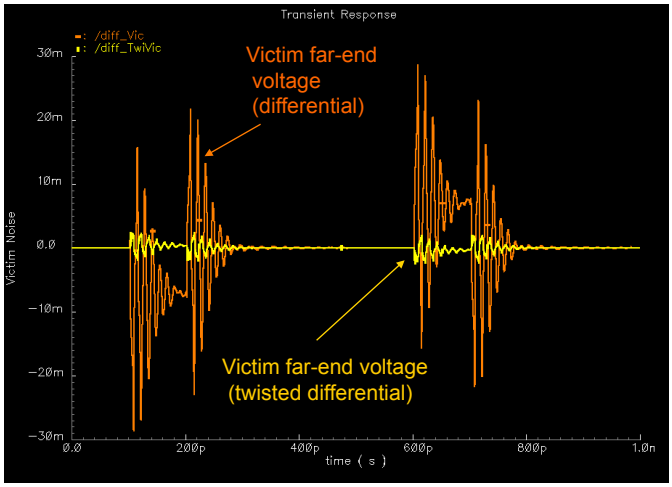
Twisted Differential Signal Lines

w = 0.6 um
t = 1.0 um
d = 1.0 um
rise time = 100 ps

L = 400 um



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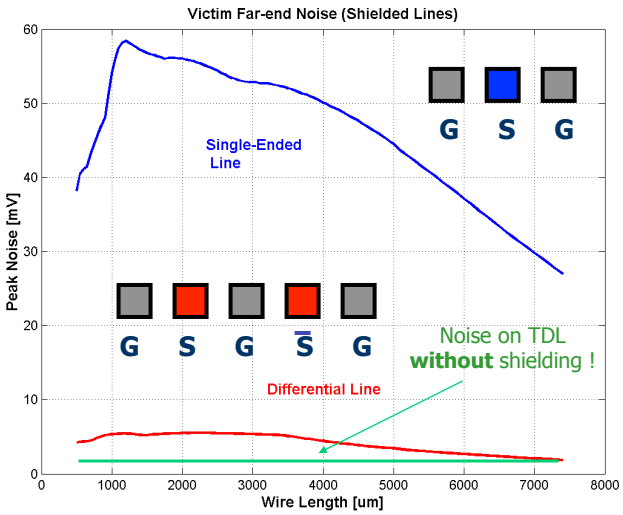
Noise Level Comparison



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