H.W-6

Prob 10.1 Given: threshold voltage of 2 precharge transistors = 2V

(i) $C = 50\,fF$

(ii) $C_D = 400\,fF$

(iii) $V(C) = V(C/2) = V_Y = 0V$ in reg^n I.

(iv) While PC is high, no other transistor is connected to D or $\bar{D}$ is on.

At steady state, there is no current flow through the pre-charging transistors.

∴ Reg I:

$$I = \frac{K}{2}(V_G - V_D - V_T)^2 = 0$$

$$V_D = V_{DD} - V_T = 5 - 2 = 3\,V$$

In region II: charge sharing occurs:

$$C_D V_D + C V(C) = C_D V_{final} + C V_{final}$$

$$V_{final} = \frac{C_D V_D + 0}{C_D + C} = \frac{400 \times 3}{400 + 50}$$

$$= 2.67V$$

10.2

(a) When bitline is driven to V_{DD}, the transistor operates in saturation region, the maximum voltage is acheived across the storage capacitor when steady state is reached.

$$I_S = \frac{1}{2} k_n (V_G - V_S - V_T)^2 = 0$$

$$V_S = 4\,V$$

(b) During READ 1 op^n, charge sharing occurs between C_S & C_{BL}:

$$C_S V_S + C_{BL} V_{BL} = (C_S + C_{BL}) V_{final}$$

$$V_{final} = \frac{C_S V_S + C_{BL} V_{BL}}{C_S + C_{BL}}$$

$$= \frac{50 \times 4 + 450 \times 2.5}{50 + 450}$$

$$= 2.65\,V$$